TM20001600
PART 2

OPERATION AND MAINTENANCE INSTRUCTION MANUAL FOR 1600 SERIES COMPUTERS (LOGIC DIAGRAMS)

Microdata™

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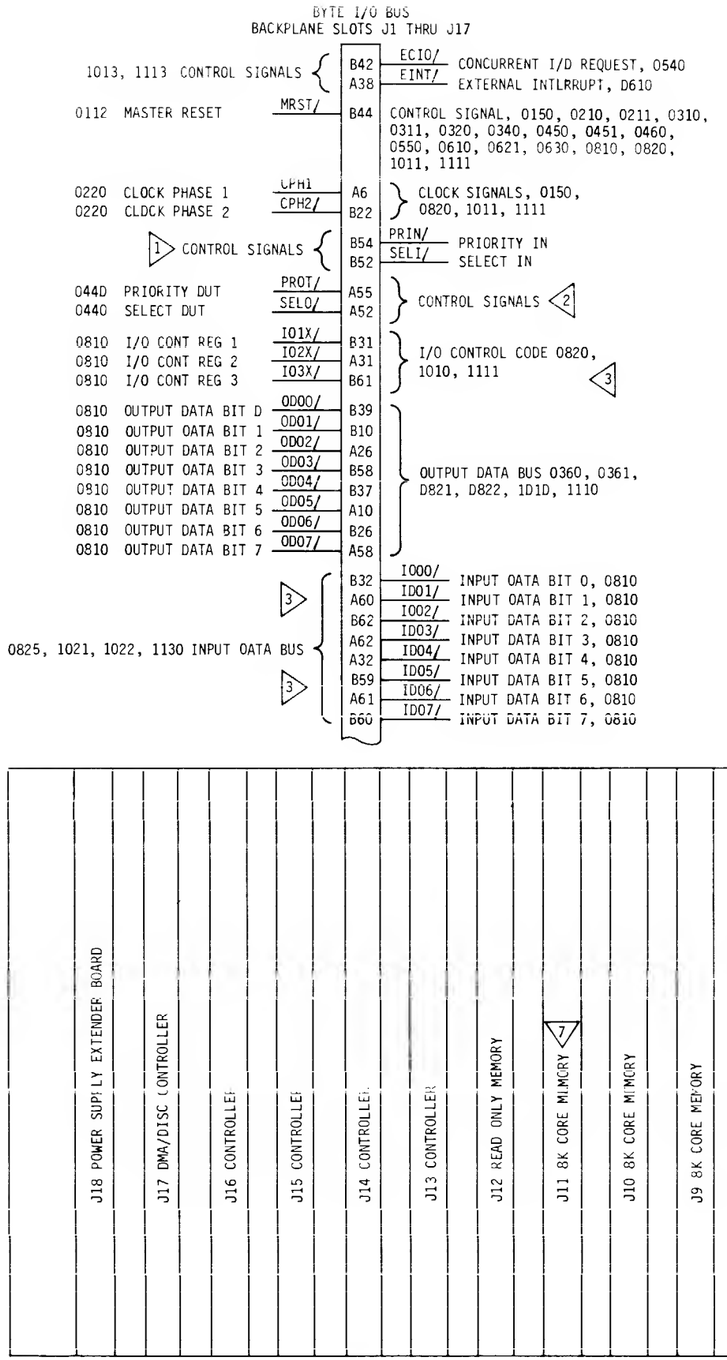
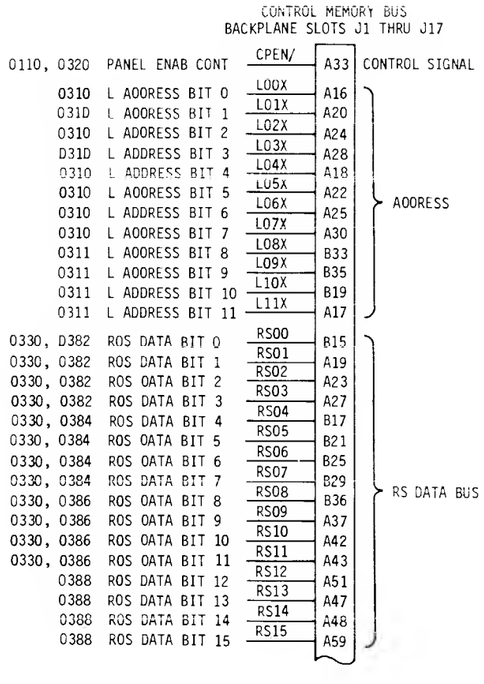
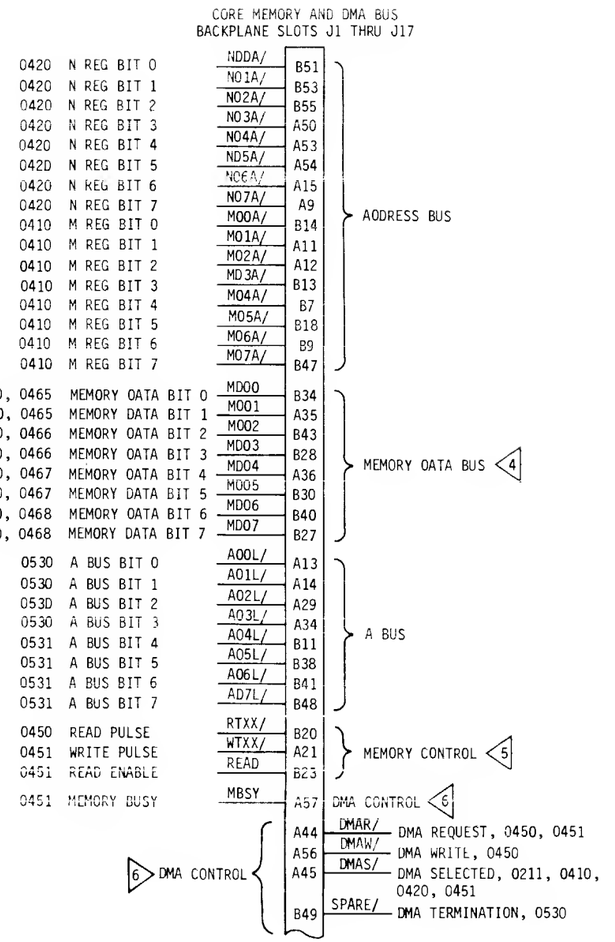
LIST OF ILLUSTRATIONS

INTERCONNECTION DIAGRAM



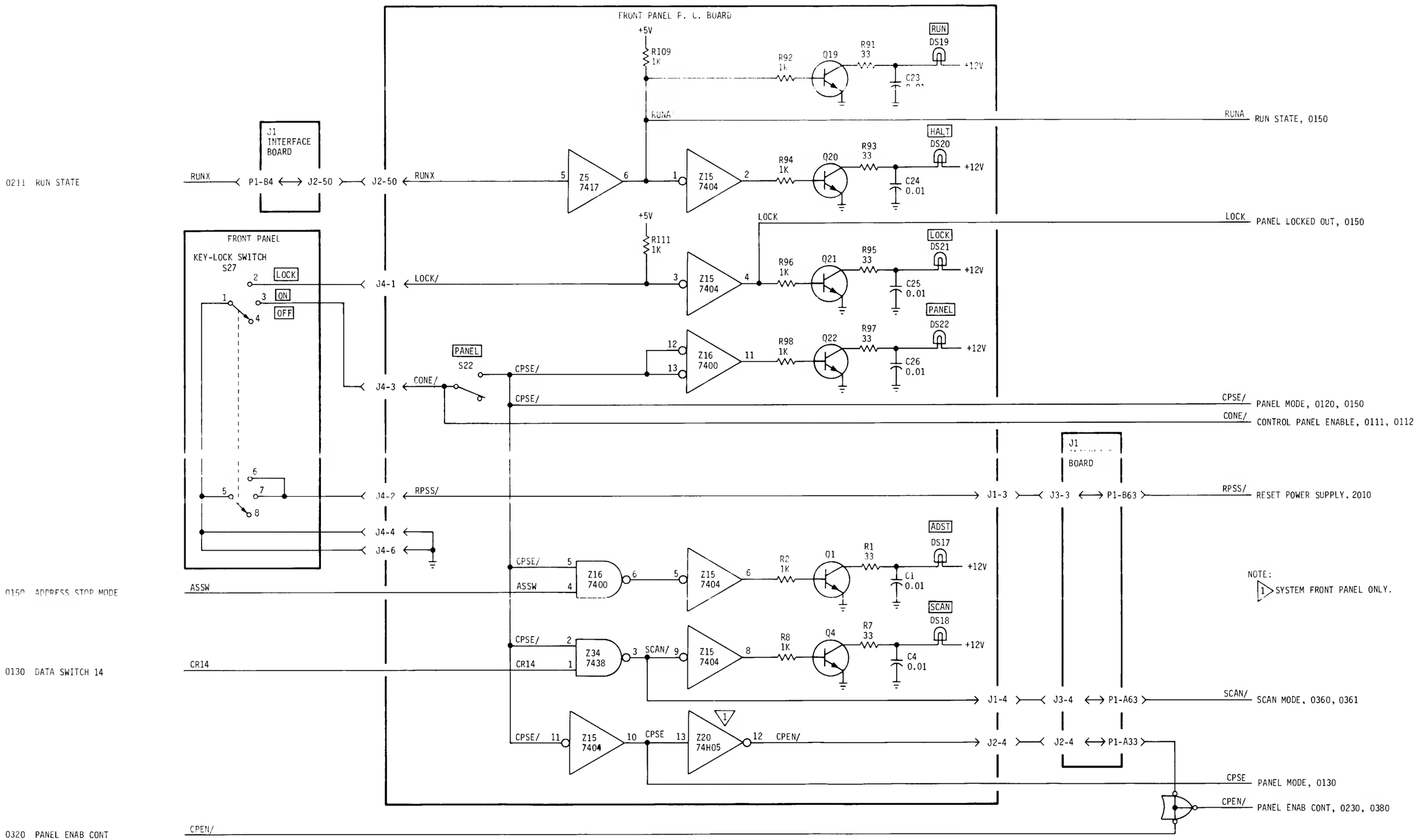




NOTES:

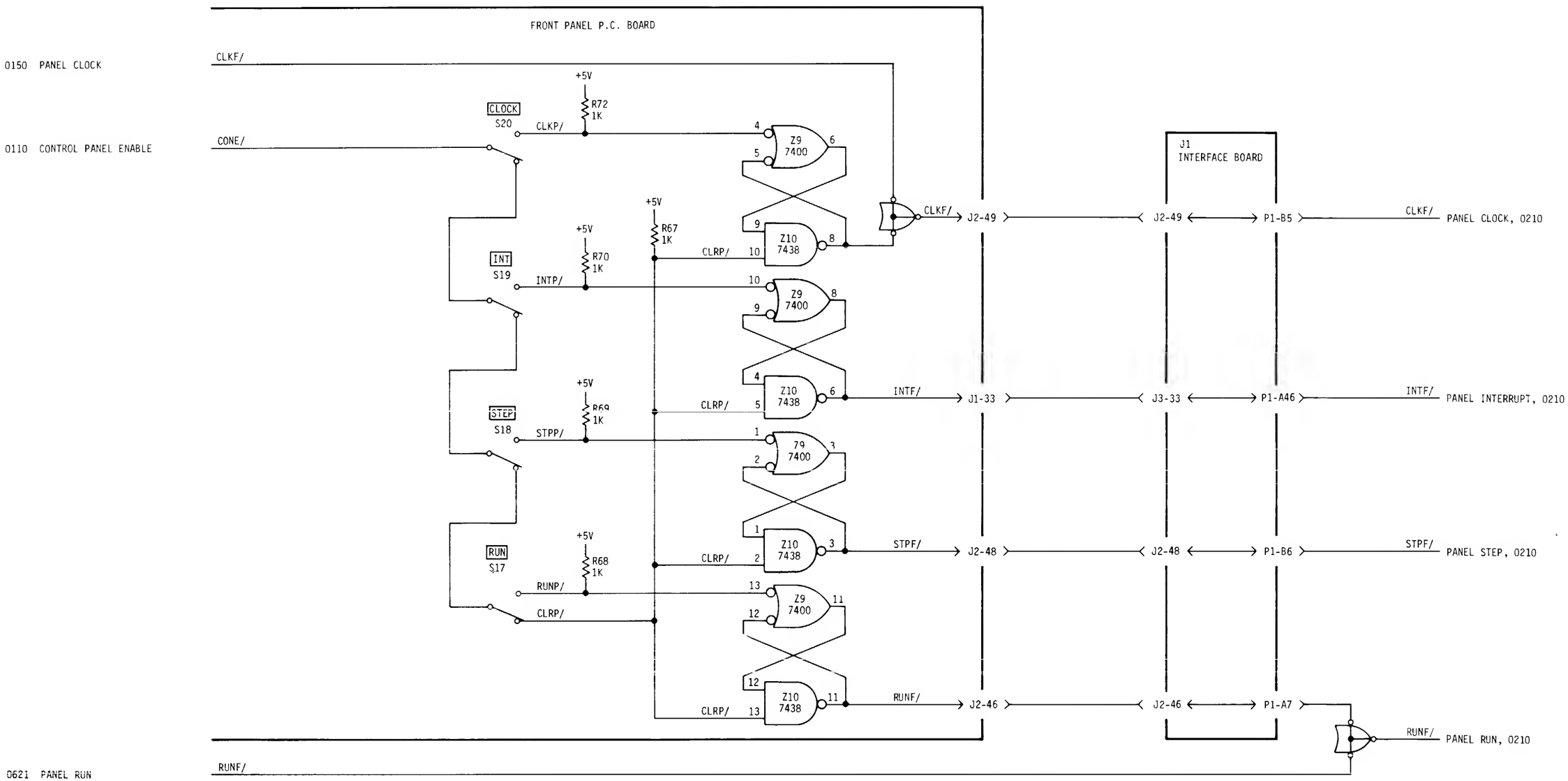
1. NOT ON J1, J2 AND J3; PINS B54 AND B52.
2. NOT ON J1, J2 ANO J17; PINS A55 AND A52.
3. NOT ON J2; PINS B61, A60, B62, A62, B59, A61 AND B60.
4. NOT ON J1 ANO J2; PINS B34, A35, B43, B28, A36, B30, B40 AND B27.
5. NOT ON J1, J12 THRU J17; PINS B20 AND A21.
6. NOT ON J1; PINS B23, A57, A44, A56, A45.
7. MEMORY SHOWN AS 64K. IF LESS THAN 64K, THE ROM, DMA, AND CONTRDLLERS MUST BE MOVED TO SLOTS ADJACENT TO THE LAST MEMORY BOARO.
8. CONTROLLER PRIORITY SEQUENCE:

	EIGHT CHANNEL CONTROLLER
	FOUR CHANNEL CONTROLLER
J13	2400 BAUD CONTROLLER
J14	MAGNETIC TAPE UNIT CONTROLLER (TWO SLOTS)
J15	PAPER TAPE CONTROLLER
J16	CARD READER CONTROLLER
	LINE PRINTER CONTROLLER



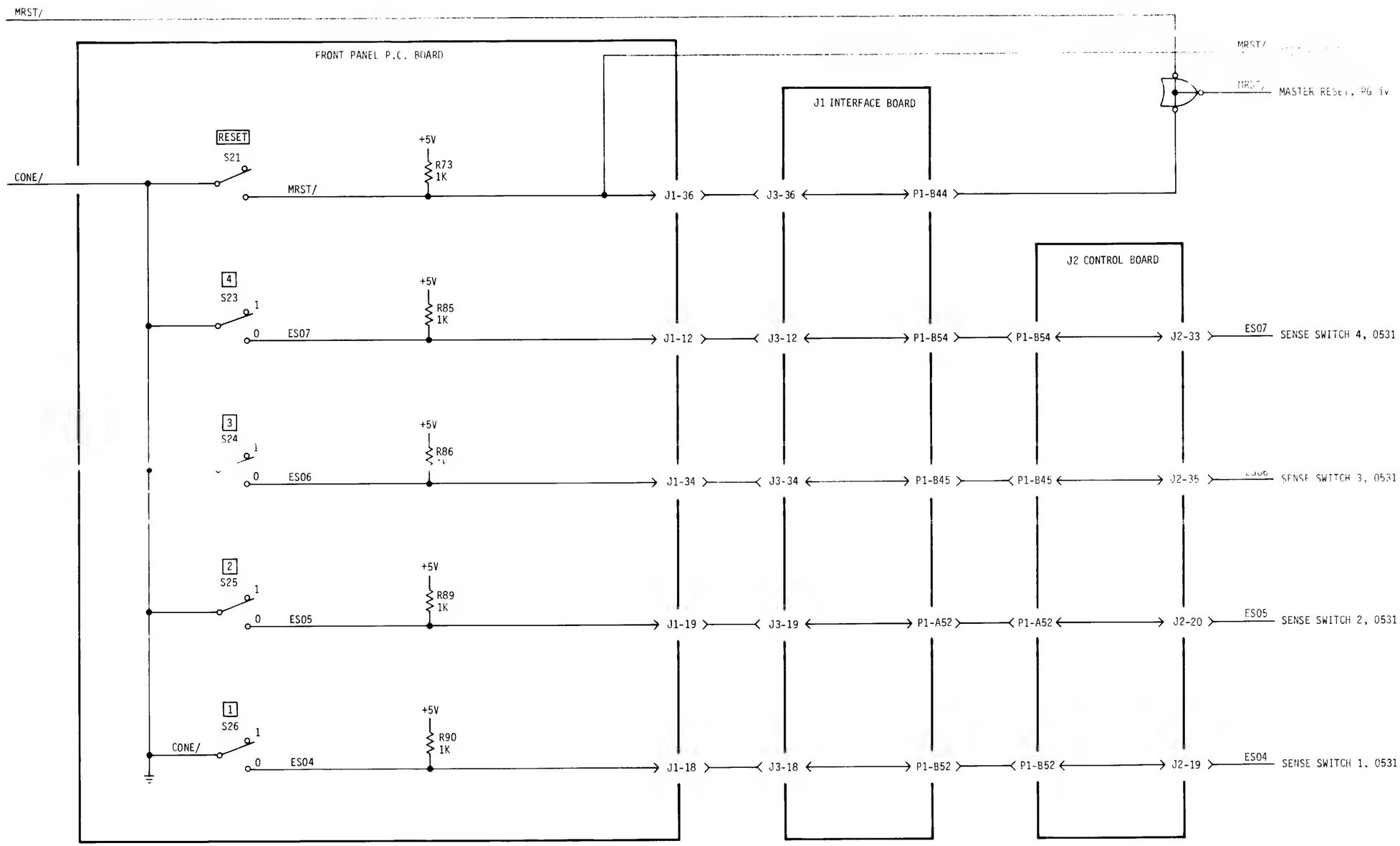
FRONT PANEL CONTROL INDICATORS

FRONT PANEL P.C. BOARD AND J1 INTERFACE BOARD 0110


FRONT PANEL P.C. BOARD
0150 PANEL CLOCK
CLKF/
0110 CONTROL PANEL ENABLE
CONE/
CLOCK
S20
CLKP/
+5V
R72
1K
Z9
7400
INT
S19
INTP/
R70
1K
R67
1K
CLRP/
Z10
7438
STEP
S18
STPP/
R69
1K
79
7400
RUN
S17
RUNP/
R68
1K
J2-49
J1-33
J2-48
J2-46
J1
INTERFACE BOARD
P1-B5
P1-A46
P1-B6
P1-A7
J3-33
PANEL CLOCK, 0210
PANEL INTERRUPT, 0210
PANEL STEP, 0210
PANEL RUN, 0210
0621 PANEL RUN
RUNF/

0621 MASTER RESET

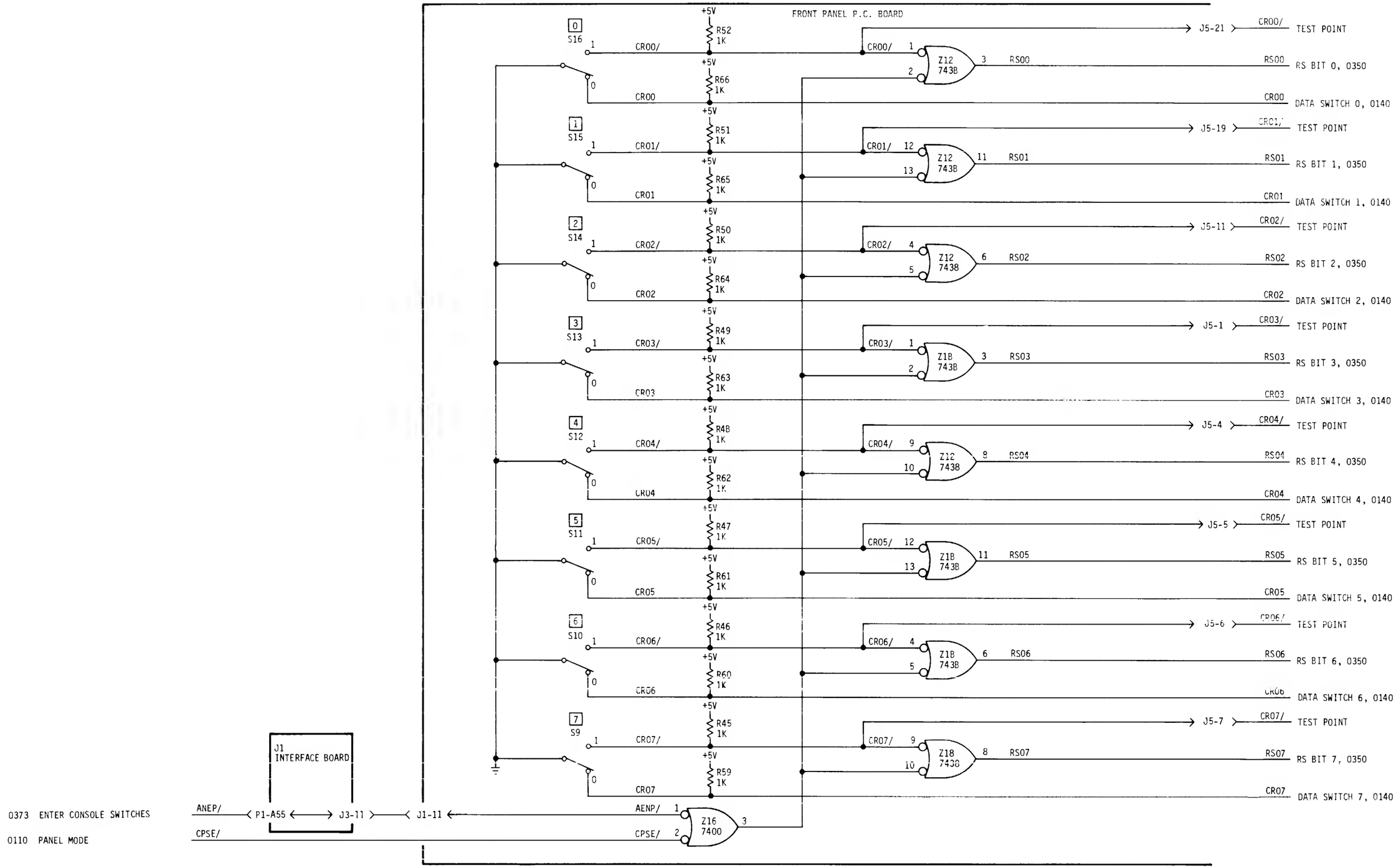
0110 CONTROL PANEL ENABLE

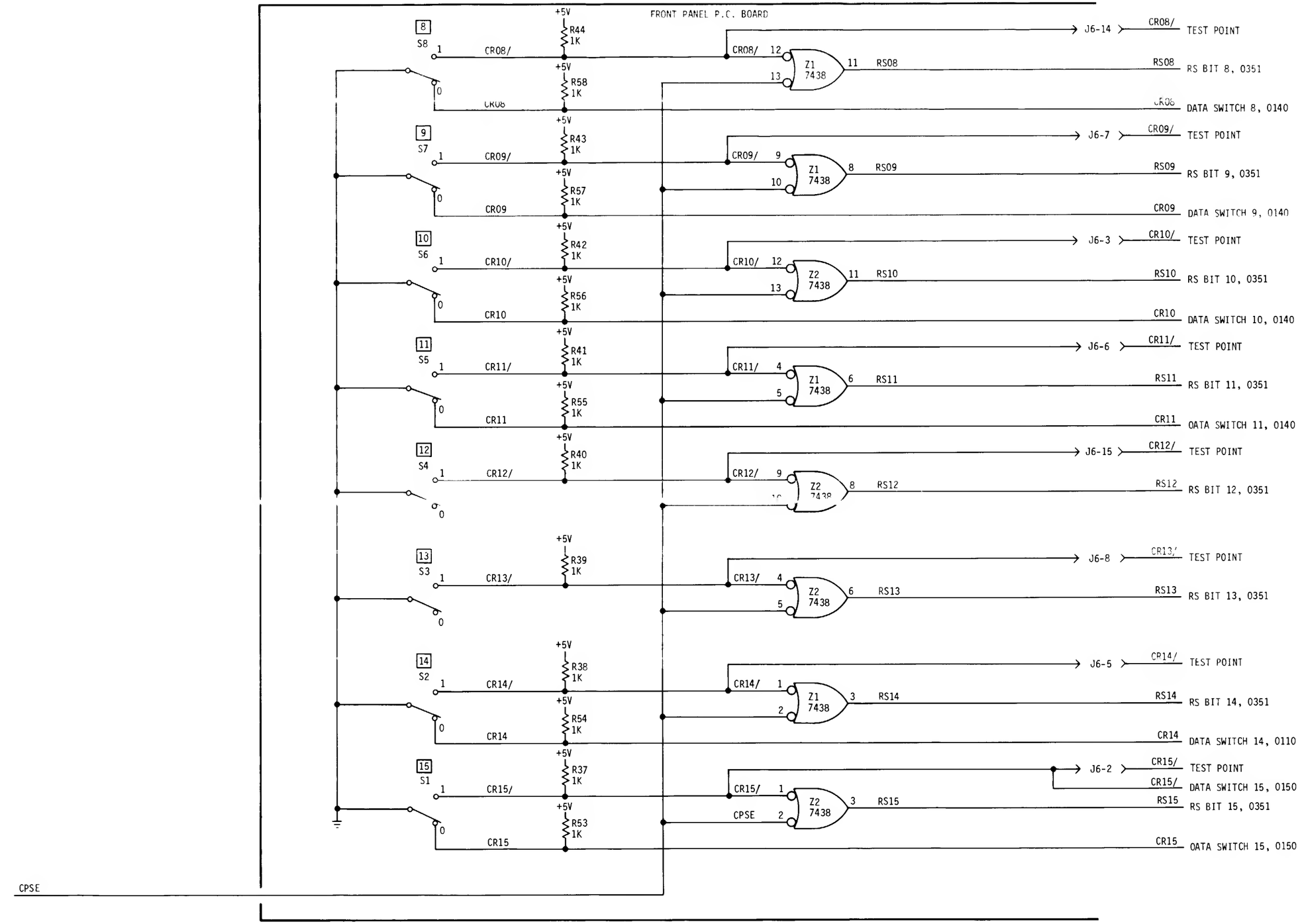


SENSE SWITCHES AND MASTER RESET

FRONT PANEL P.C. BOARD, J1 INTERFACE BOARD
AND J2 CONTROL BOARD
0112

LOWER DATA SWITCHES

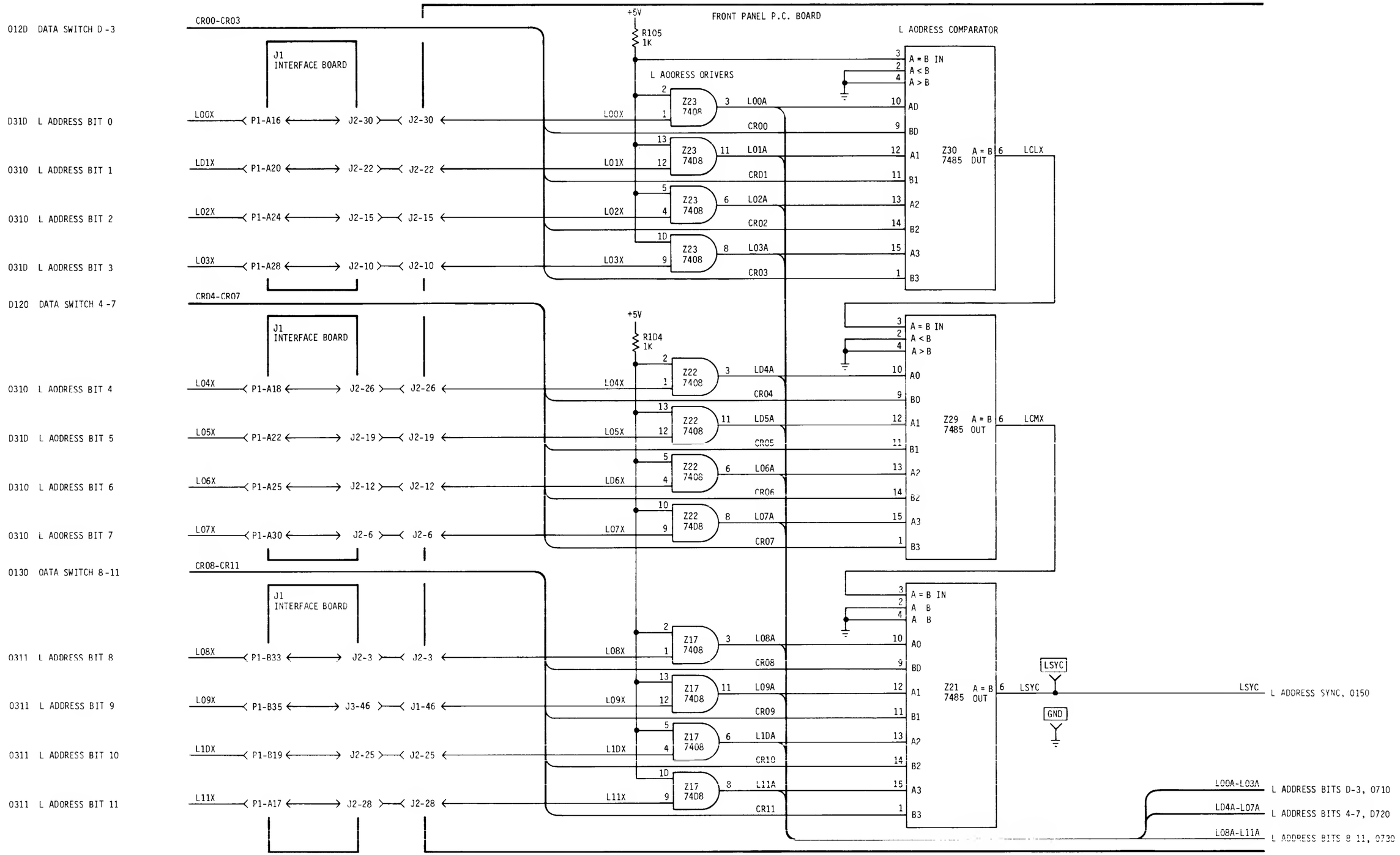


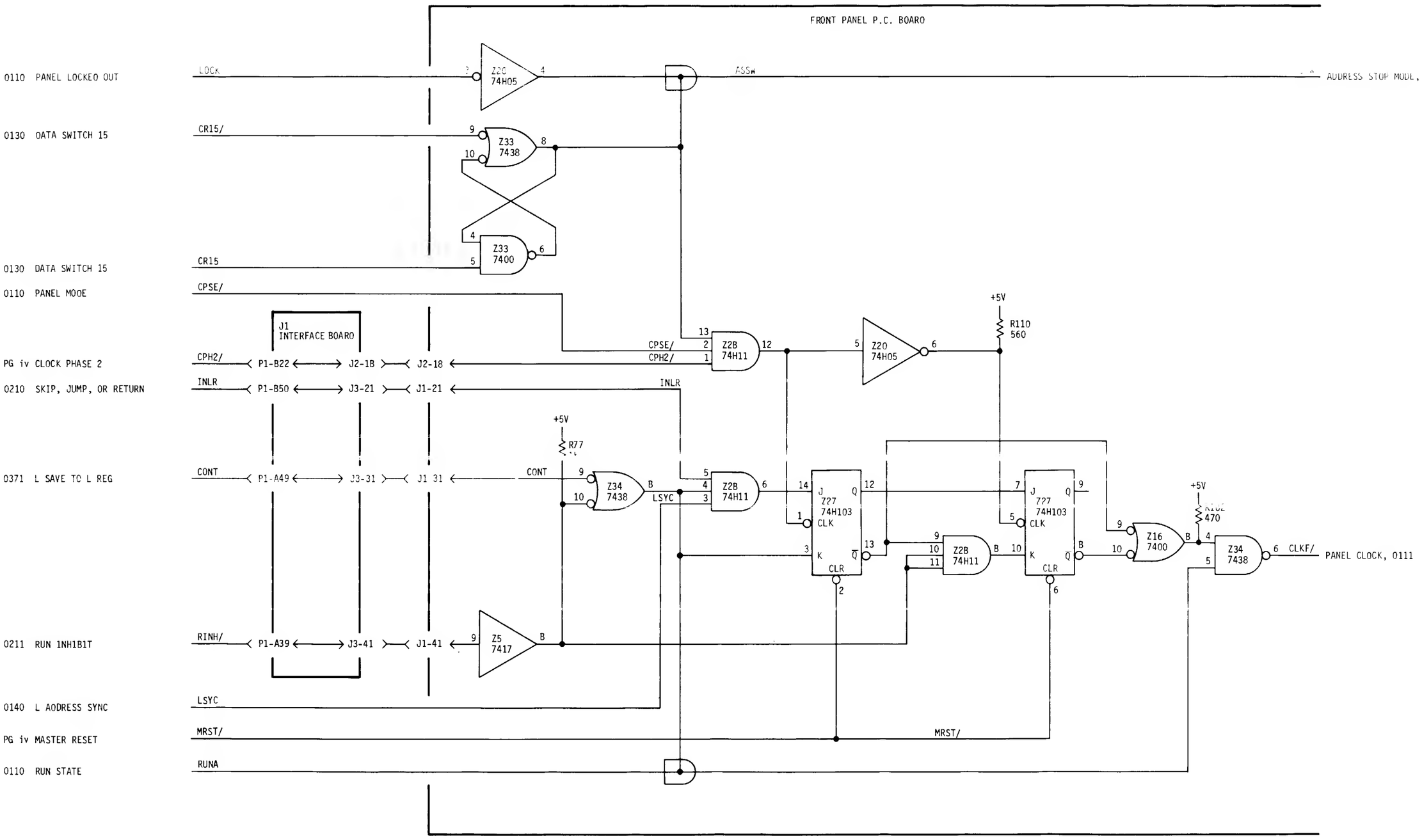


UPPER DATA SWITCHES

FRONT PANEL P.C. BOARD
0130

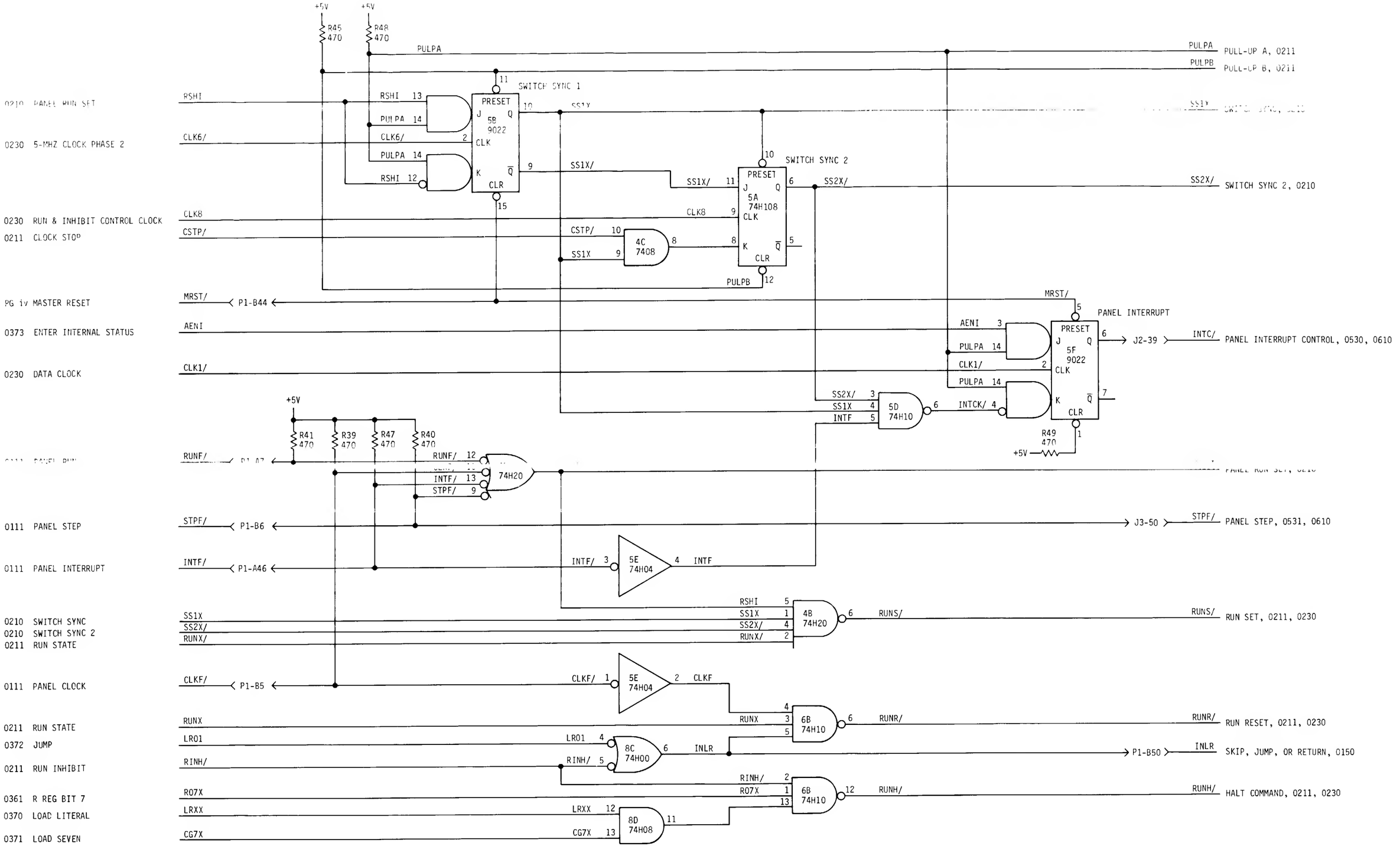
L ADDRESS DRIVERS AND COMPARATOR





ADDRESS STOP LOGIC

FRONT PANEL P.C. BOARD
AND J1 INTERFACE BOARD
0150



RUN AND INHIBIT CONTROL 1

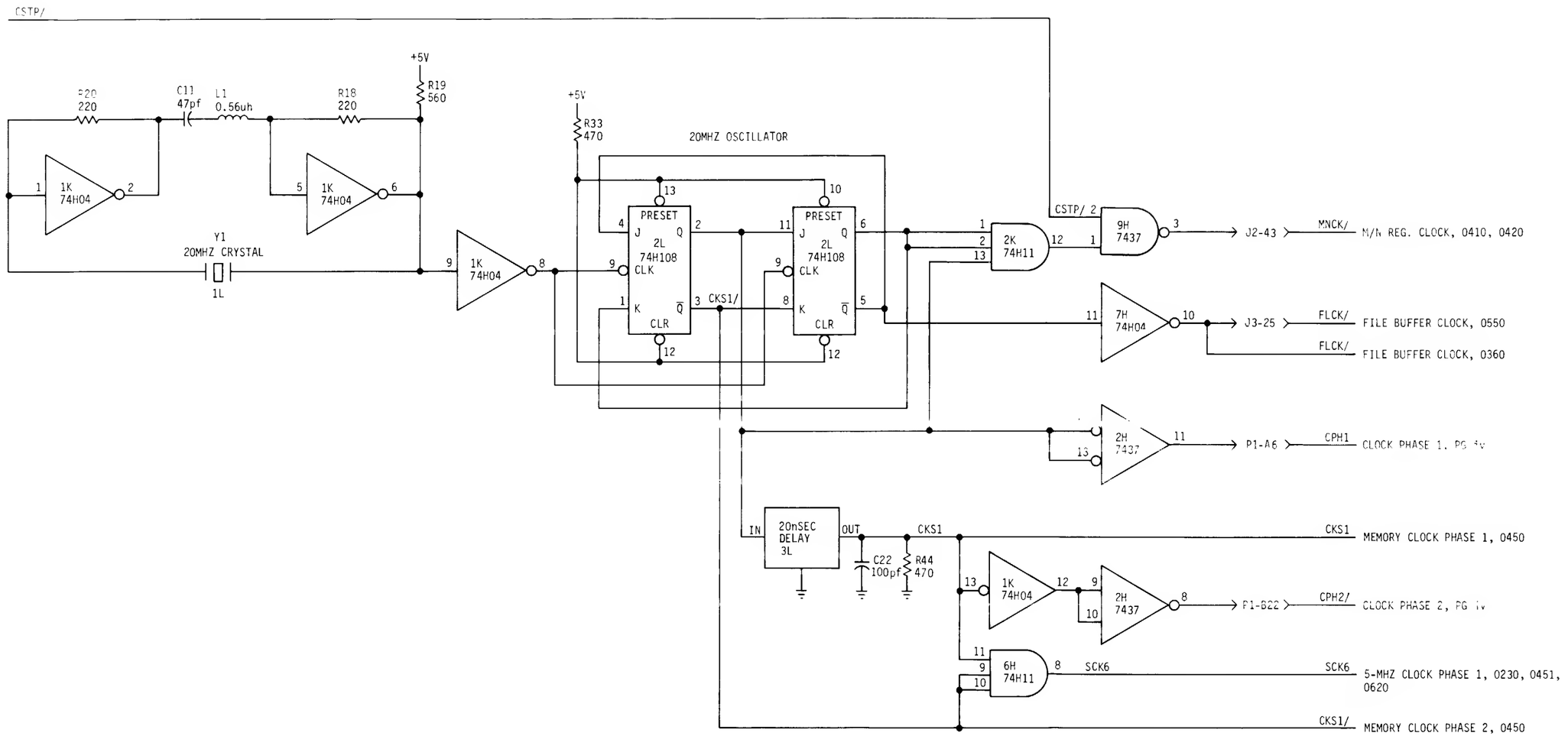
J2 CONTROL BOARD
0210

RUN AND INHIBIT CONTROL 2

PG iv MASTER RESET
0210 RUN RESET
0210 HALT COMMAND
0230 5-MHZ CLOCK PHASE 2
0210 PULL-UP A
0210 RUN SET
0210 PULL-UP B
0230 RUN & INHIBIT CONTROL CLOCK
0372 "UMP"
0370 COMPARE FILE
0520 HIGH-ORDER BIT CARRY
0370 "AXX/" TEST IF NOT ZERO
0570 A BUS ZERO DECODE
0370 TEST IF ZERO
0211 CLOCK STOP
0450 MEMORY READ OR WRITE
0451 MEMORY STOP
0372 M 09 1 REG SELECT
0451 MEMORY BUSY INTERNAL
PG iv DMA SELECTED
0372 T 42" TRANSFER T. B BUS
0451 MEMORY DATA NOT AVAILABLE

MRST/ P1-B44
RUNR/
RUNH/
7F 74H00
CLK6/
PULPA
RUNS/
PULPB
5B 9022 PRESET CLK K Q CLR
MRST/
RUNX/
RUNX
RUNX/ RUN STATE, 0210, 0230, 0620
P1-B4
RUNX RUN STATE, 0110
8C 74H00
RINH/
7C 7438
CSTP/ CLOCK STOP, 0211, 0630
5A 74H108 PRESET J Q CLK K Q CLR
RINH/
P1-A39
RINH/ RUN INHIBIT, 0150
RINH/ RUN INHIBIT, 0210, 0220, 0372
CLK8
LRO1/
CPXX
CRY7
J3-49
6K 74H00
6J 76H20
RINK
TNXX/
6L 74H04
AZO7/
RIN3
+5V
R51 220
TZXX/
CSTP/
MNXX
MSTP
MNRX
MBYI
DMAS/ P1-A45
BTXR J2-31
MDNA
2J 74H11
TMCE
7H 74H04
2H 7437
CSTP
CLOCK STOP, 0230
CSTP/ CLOCK STOP, 0210, 0220, 0230, 0360, 0372, 0450
TMCE TM CLOCK ENABLE, 0230

0211 CLOCK STOP

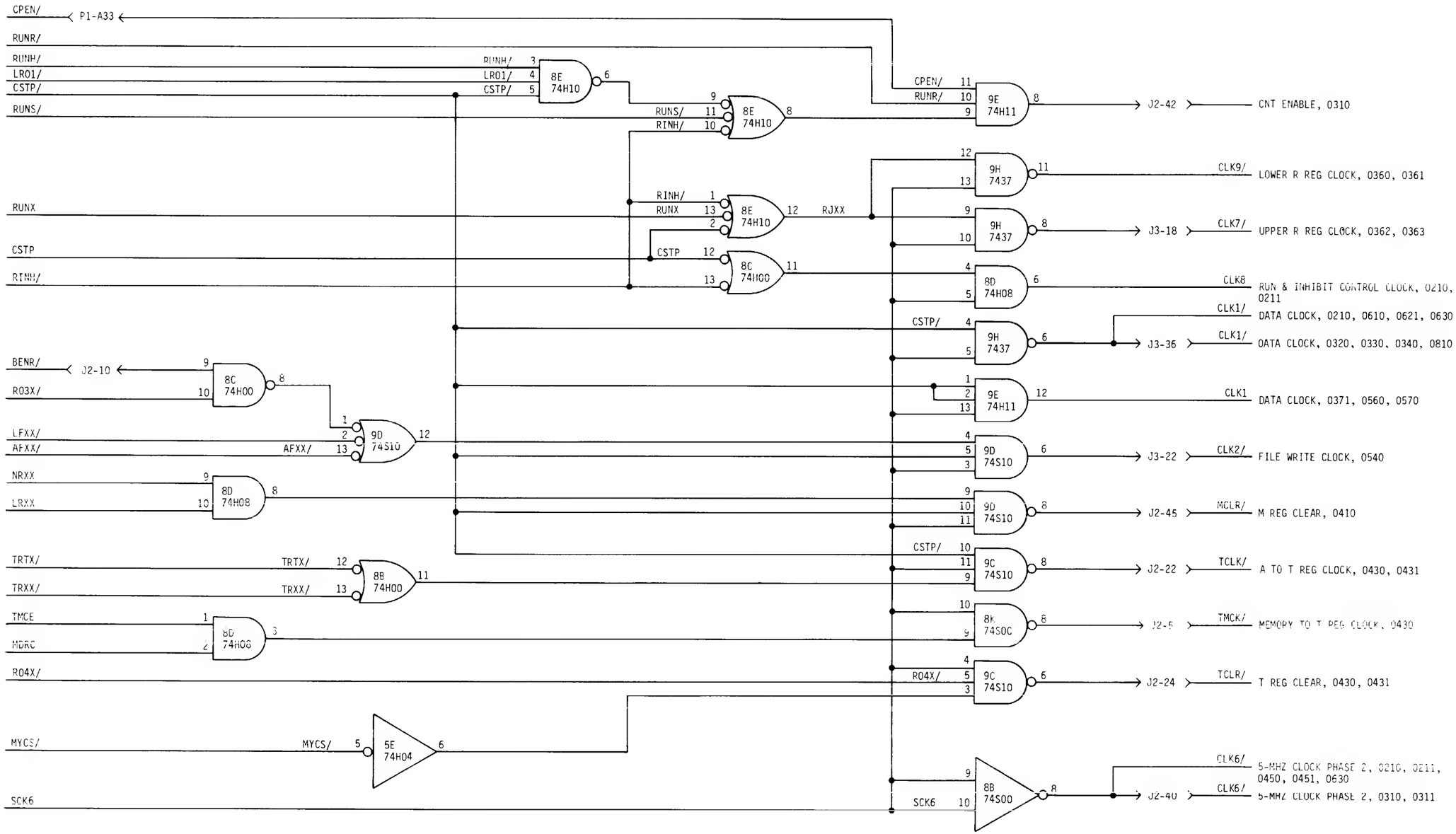


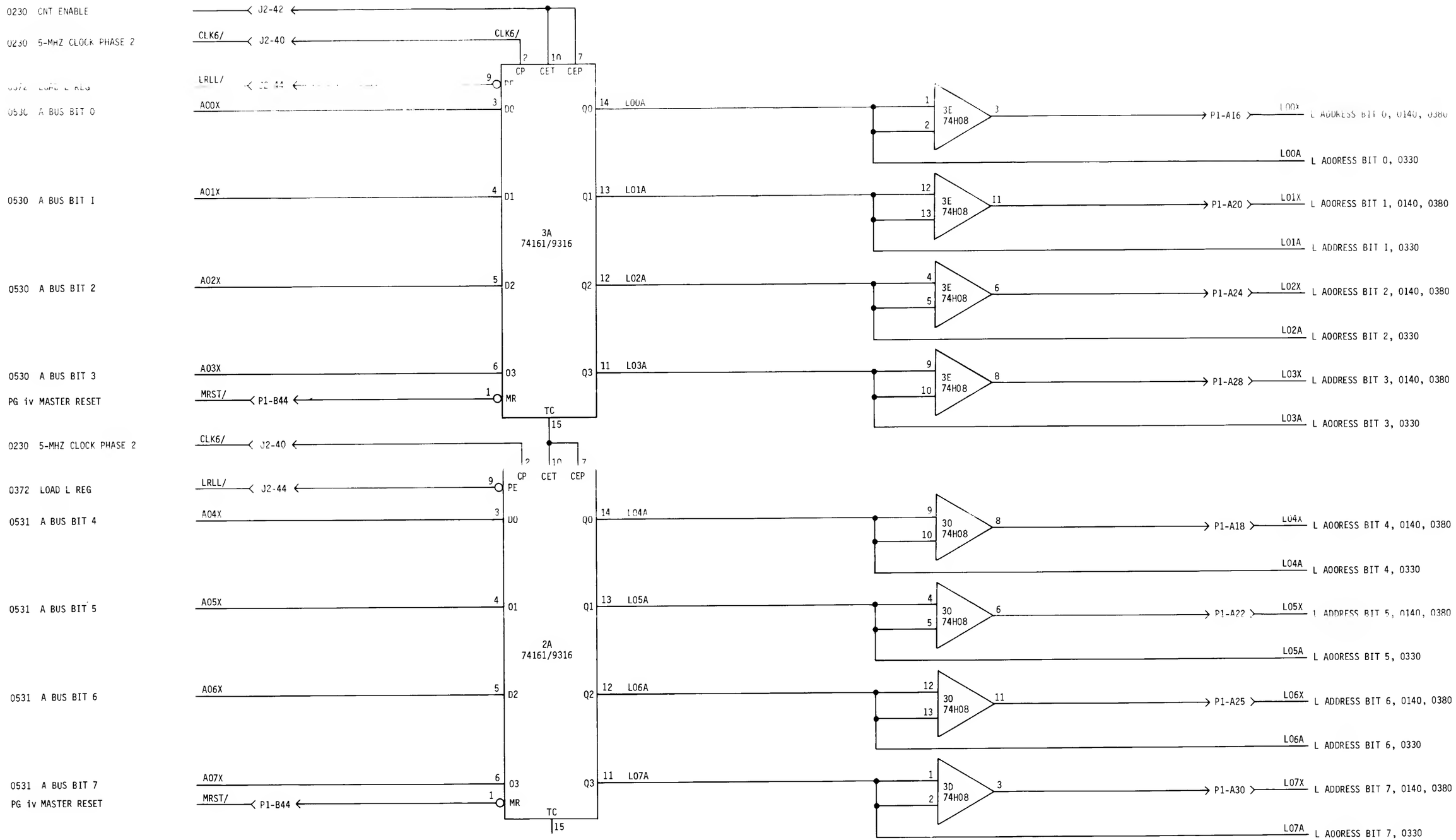
CLOCK GENERATOR

J2 CONTROL BOARD
0220

CLOCK GATES

0110 PANEL ENAB CONT
0210 RUN RESET
0210 HALT COMMAND
0372 JUMP
0211 CLOCK STOP
0210 RUN SET
0211 RUN STATE
0211 CLOCK STOP
0211 RUN INHIBIT
0374 R REG TO B BUS
0360 R REG BIT 3
0370 LOAD FILE
0370 ADD FILE
0371 LOAD N
0370 LOAD LITERAL
0371 RETURN, LOAD T
0371 LOAD T
0211 TM CLOCK ENABLE
0451 READ MEMORY DATA
0361 R REG BIT 4
0450 MEMORY CYCLE START
0220 5-MHZ CLOCK PHASE 1

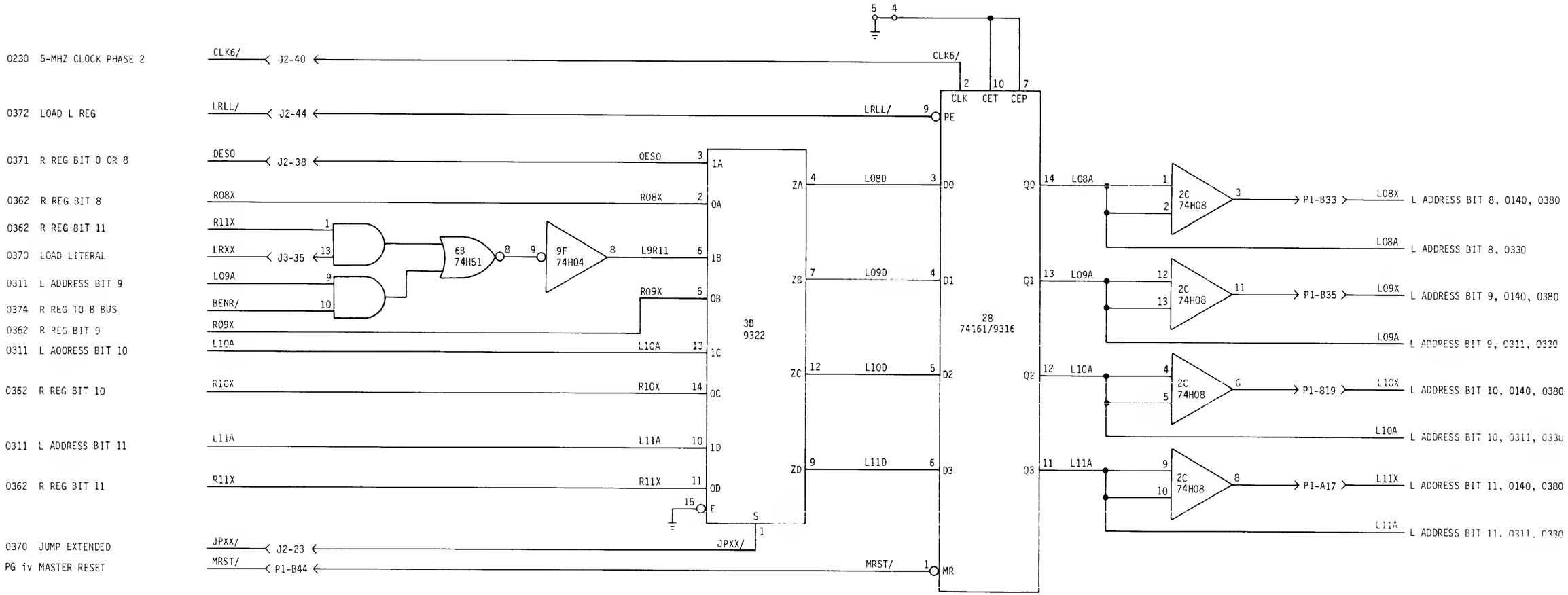


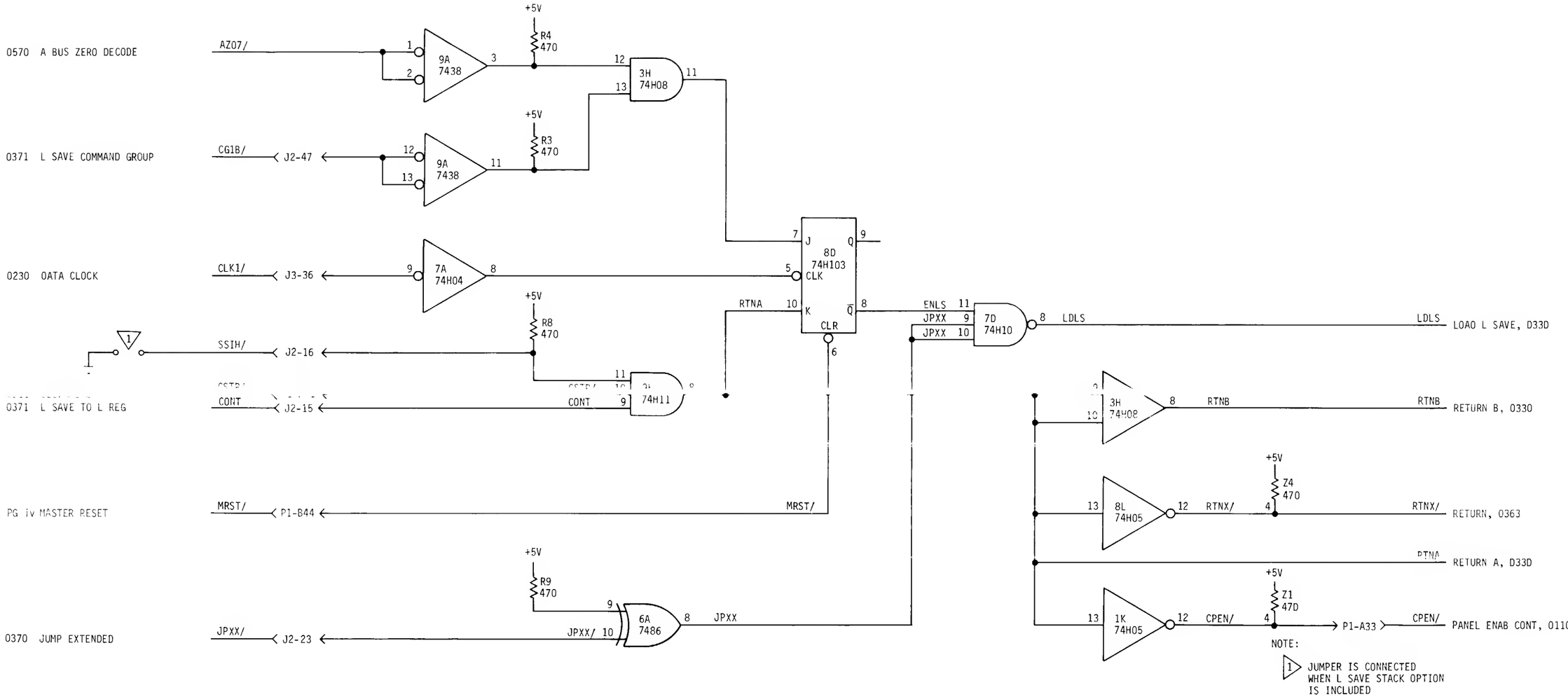


L REGISTER BITS 0-7

J3 DATA BOARD
0310

L REGISTER BITS 8-11





L SAVE CONTROL

J3 DATA BOARD
0320

L SAVE REGISTER

0320 RETURN B

0310 L ADDRESS BIT 0

0310 L ADDRESS BIT 1

0310 L ADDRESS BIT 2

0310 L ADDRESS BIT 3

0230 DATA CLOCK

0320 LOAD L SAVE

0550 PULL-UP 1

0310 L ADDRESS BIT 4

0310 L ADDRESS BIT 5

0310 L ADDRESS BIT 6

0310 L ADDRESS BIT 7

0230 DATA CLOCK

0320 LOAD L SAVE

0550 PULL-UP 1

0311 L ADDRESS BIT 8

0311 L ADDRESS BIT 9

0311 L ADDRESS BIT 10

0311 L ADDRESS BIT 11

0230 DATA CLOCK

0320 LOAD L SAVE

0550 PULL-UP 1

0320 RETURN A

RTNB

L00A 22 D3 Q3 23 — 2F 74H04 (11→10) — LS00/ 4,5 — 1J 7438 (6) → P1-B15 → RS00 RS BIT 0, 0350

L01A 20 D2 Q2 21 — 2F 74H04 (3→4) — LS01/ 4,5 — 1H 7438 (6) → P1-A19 → RS01 RS BIT 1, 0350

L02A 18 D1 Q1 19 — 2E 74H04 (13→12) — LS02/ 12,13 — 1H 7438 (11) → P1-A23 → RS02 RS BIT 2, 0350

L03A 16 D0 Q0 17 — 2E 74H04 (1→2) — LS03/ 1,2 — 1H 7438 (3) → P1-A27 → RS03 RS BIT 3, 0350

3F 9308

CLK1/ ← J3-36 ← 14 ; LOLS 15 ; E

MR ← PUL1 13

L04A 10 D3 Q3 11 — 2E 74H04 (9→8) — LS04/ 9,10 — 1H 7438 (8) → P1-B17 → RS04 RS BIT 4, 0350

L05A 8 D2 Q2 9 — 2E 74H04 (5→6) — LS05/ 9,10 — 1J 7438 (8) → P1-B21 → RS05 RS BIT 5, 0350

L06A 6 D1 Q1 7 — 2F 74H04 (5→6) — LS06/ 1,2 — 1J 7438 (3) → P1-B25 → RS06 RS BIT 6, 0350

3F 9308

L07A 4 D0 Q0 5 — 2F 74H04 (3→4) — LS07/ 12, RTNB 13 — 1J 7438 (11) → P1-B29 → RS07 RS BIT 7, 0350

CLK1/ ← J3-36 ← 2 ; LDLS 3 ; E

MR ← PUL1 1

L08A 10 D3 Q3 11 — 2F 74H04 (11→10) — LS08/ 4, RTNA 5 — 1L 7438 (6) → P1-B36 → RS08 RS BIT 8, 0362 ; RS09 RS BIT 8, 0351

L09A 8 D2 Q2 9 — 2F 74H04 (1→2) — LS09/ 1,2 — 1L 7438 (3) → P1-A37 → RS09 RS BIT 9, 0362 ; RS09 RS BIT 9, 0351

2D 9308

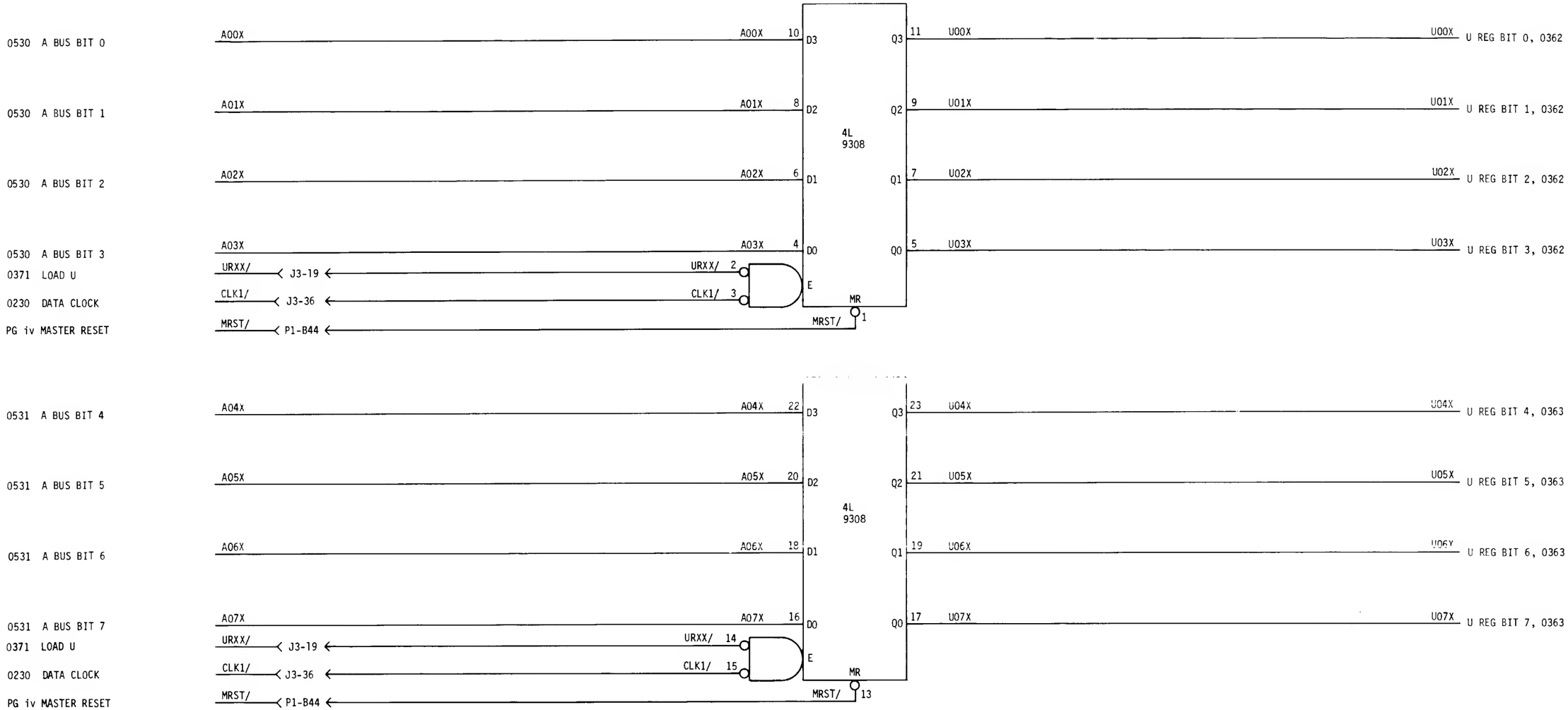
L10A 6 D1 Q1 7 — 2F 74H04 (13→12) — LS10/ 12,13 — 1L 7438 (11) → P1-A42 → RS10 RS BIT 10, 0362 ; RS10 RS BIT 10, 0351

L11A 4 D0 Q0 5 — 2F 74H04 (9→8) — LS11/ 9, RTNA 10 — 1L 7438 (8) → P1-A43 → RS11 RS BIT 11, 0362 ; RS11 RS BIT 11, 0351

CLK1/ ← J3-36 ← 2 ; 3 ; E

MR ← PUL1 1

RTNA



U REGISTER

J3 DATA BOARD
0340

RS BUS AND DRIVERS

0382 ROS DATA BIT 0
0330 RS BIT 0

0382 ROS DATA BIT 1
0330 RS BIT 1

0382 ROS DATA BIT 2
0330 RS BIT 2

0382 ROS DATA BIT 3
0330 RS BIT 3

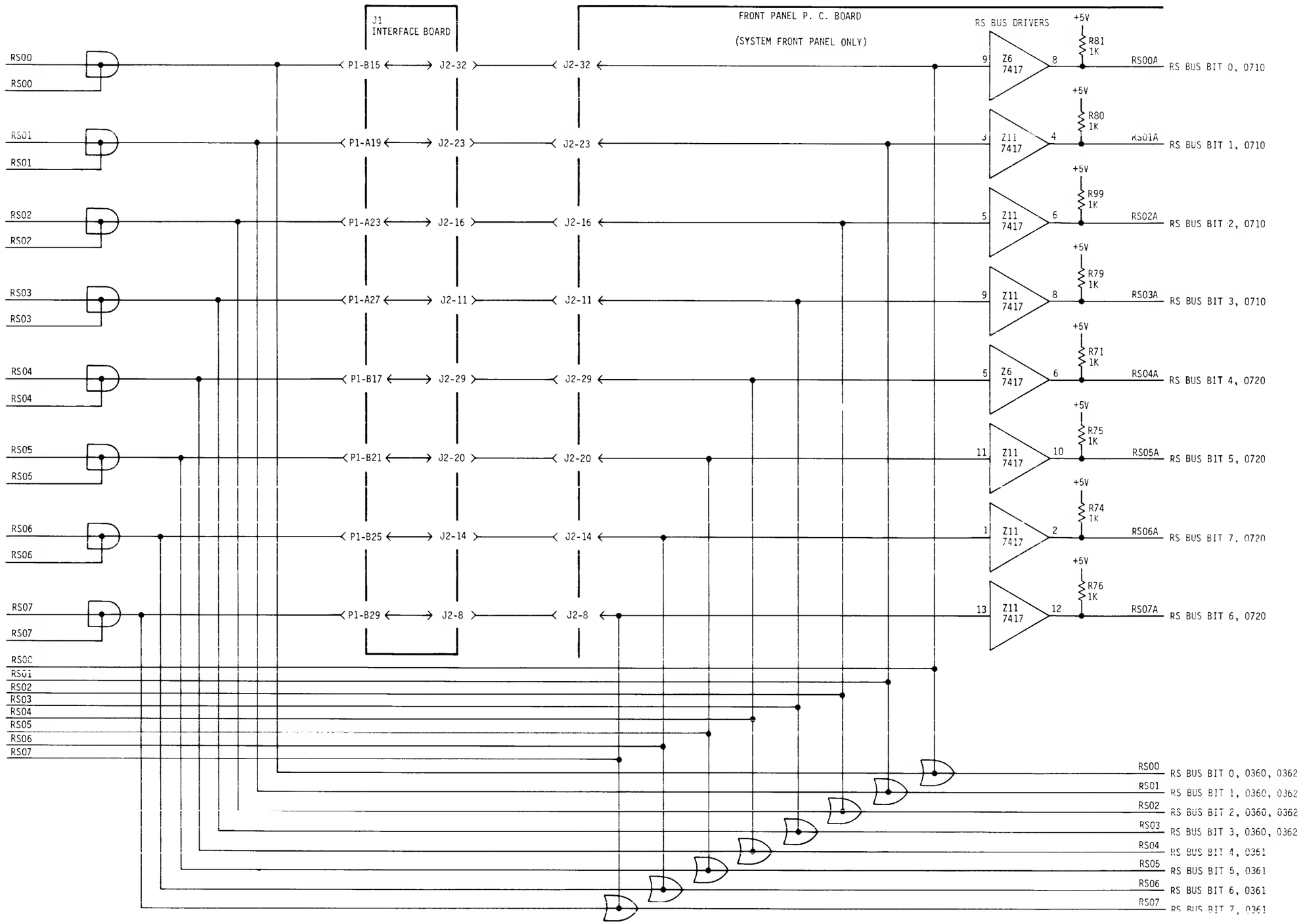
0384 ROS DATA BIT 4
0330 RS BIT 4

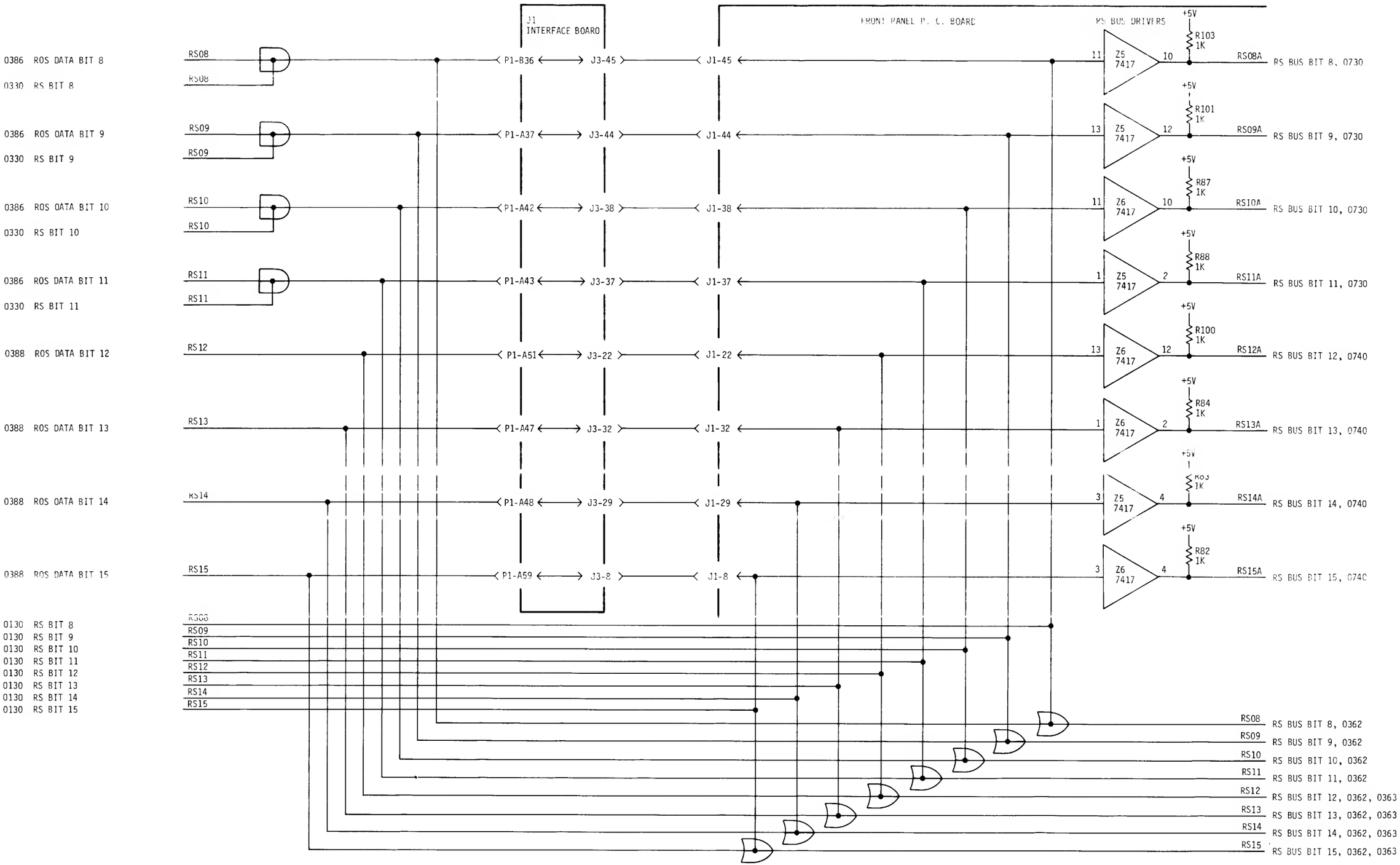
0384 ROS DATA BIT 5
0330 RS BIT 5

0384 ROS DATA BIT 6
0330 RS BIT 6

0384 ROS DATA BIT 7
0330 RS BIT 7

0120 RS BIT 0
0120 RS BIT 1
0120 RS BIT 2
0120 RS BIT 3
0120 RS BIT 4
0120 RS BIT 5
0120 RS BIT 6
0120 RS BIT 7





RS BUS AND DRIVERS

FRONT PANEL P.C. BOARD
0351

LOWER R REGISTER BITS 0-3

0220 FILE BUFFER CLOCK
0211 CLOCK STOP
FLCK/
CSTP/
6H 74H11
ENABLE MODIFY LOWER, 0361

0371 MODIFY LOWER COMMAND
JUXX/
5H 74H04

PG iv OUTPUT DATA BIT 0
DD00/
P1-B39
1E 7438
ODDD/
+5V
R31 470
R32 470
0350 PS BUS BIT 0
RS00
P1-B15
RS00
PRESET
2E 74H74
CLR
SCAN/
R00X
R00X/
J3-37
R REG BIT 0, 0371
R REG BIT 0, 0560
R REG BIT 0, 0510

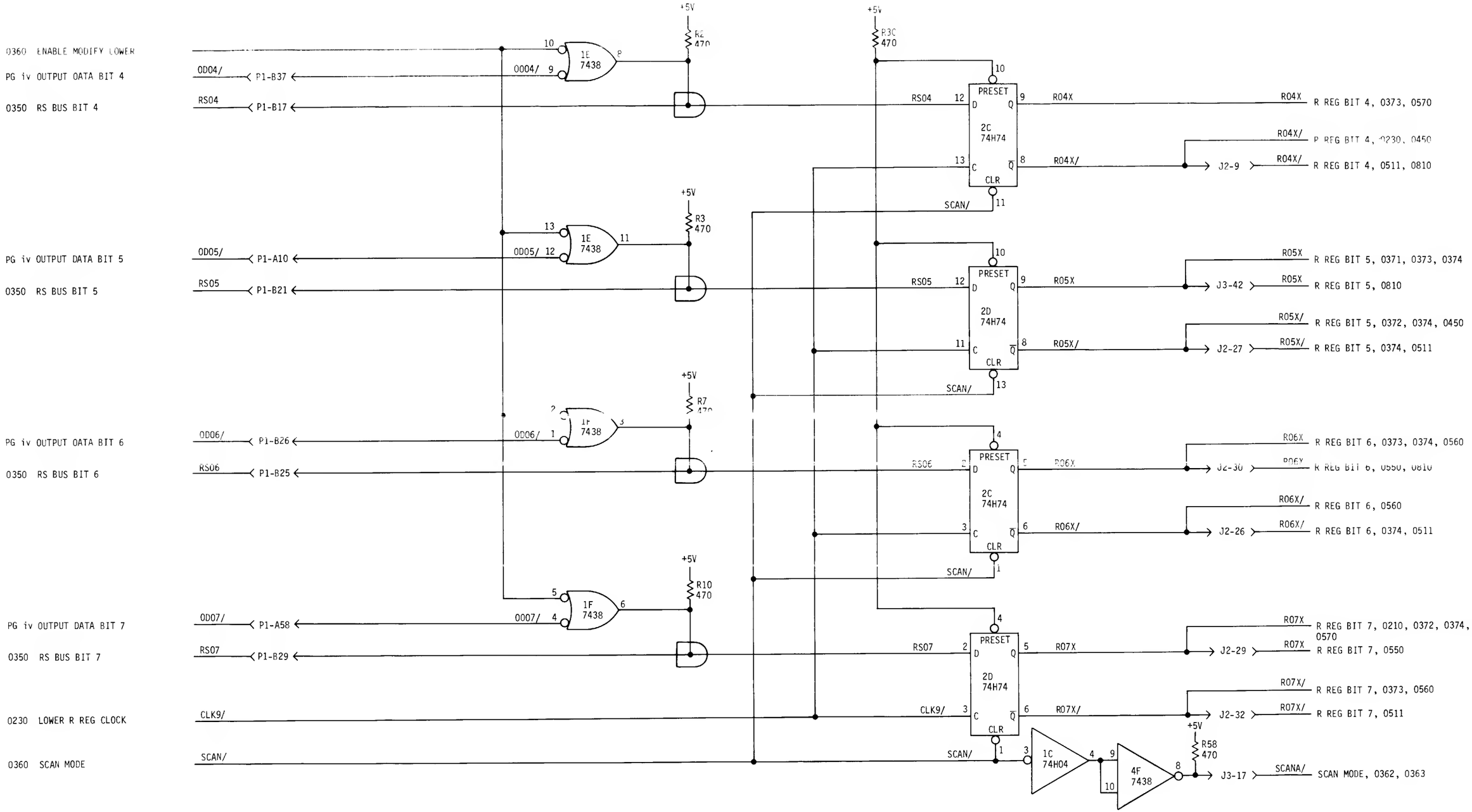
PG iv OUTPUT DATA BIT 1
OD01/
P1-B10
1E 7438
OD01/
+5V
R28 470
R6 47D
0350 RS BUS BIT 1
RS01
P1-A19
RS01
2F 74H74
R01X
R01X/
J3-39
R REG BIT 1, 0371
R REG BIT 1, 0560
R REG BIT 1, 0510

PG iv OUTPUT DATA BIT 2
OD02/
P1-A26
1F 7438
OD02/
+5V
R29 470
0350 RS BUS BIT 2
RS02
P1-A23
RS02
2E 74H74
R02X
R02X/
J3-41
R REG BIT 2, 0371
R REG BIT 2, 0560
R REG BIT 2, 0510

PG iv OUTPUT DATA BIT 3
OD03/
P1-B58
1F 7438
OD03/
+5V
R8 470
0350 RS BUS BIT 3
RS03
P1-A27
RS03
2F 74H74
R03X
R03X/
J3-43
R REG BIT 3, 0230
R REG BIT 3, 0510

0230 LOWER R REG CLOCK
CLK9/

0110 SCAN MODE
SCAN/
P1-A68
SCAN/
SCAN MODE, 0361



LOWER R REGISTER BITS 4-7

J2 CONTROL BOARD
0361

UPPER R REGISTER BITS 8-11

0361 SCAN MODE

0330 RS BIT 8
0351 RS BUS BIT 8

0340 U REG BIT 0

0230 UPPER R REG CLOCK

0330 RS BIT 9
0351 RS BUS BIT 9

0340 U REG BIT 1

0330 RS BIT 10
0351 RS BUS BIT 10

0340 U REG BIT 2

0330 RS BIT 11
0351 RS BUS BIT 11

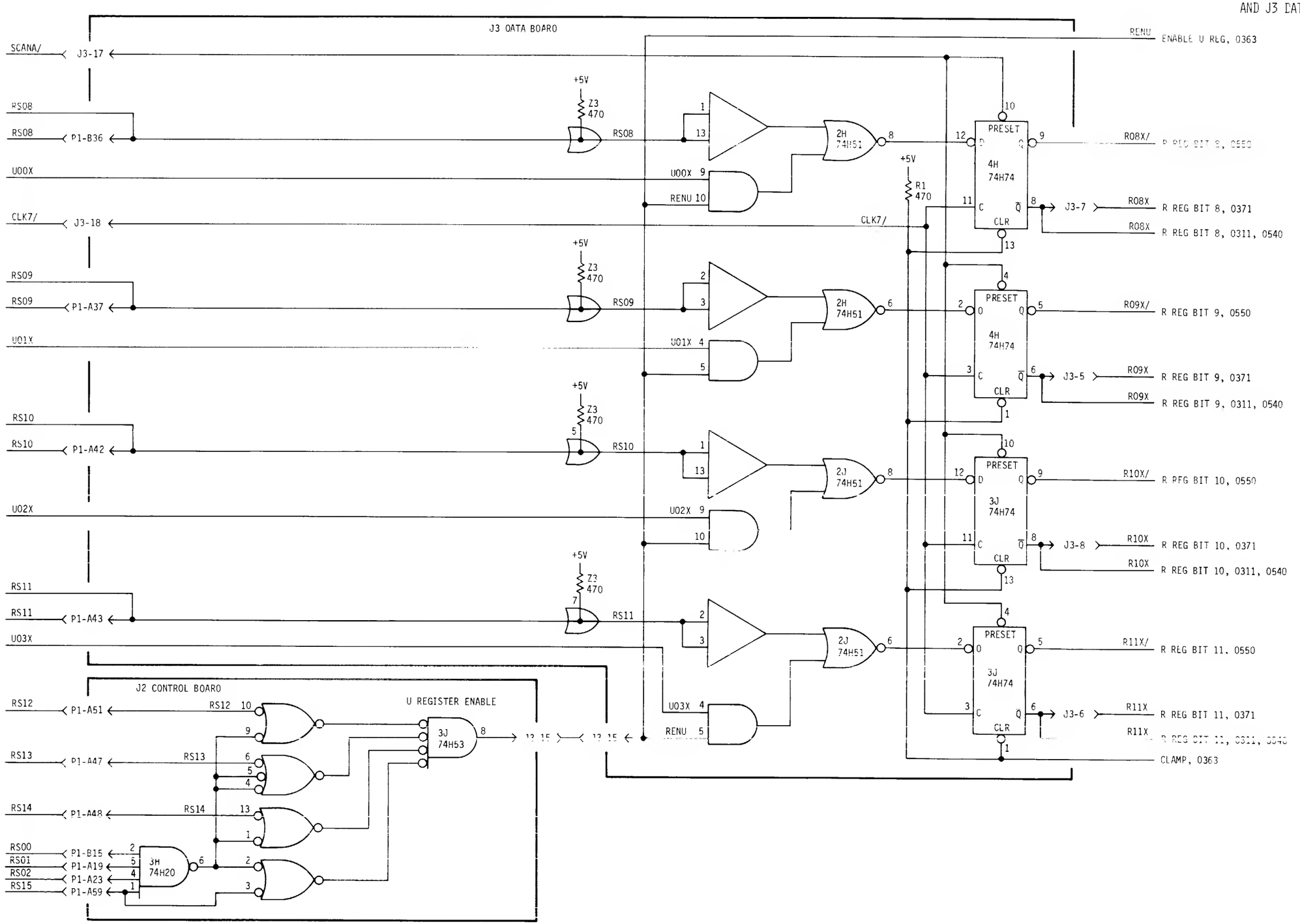
0340 U REG BIT 3

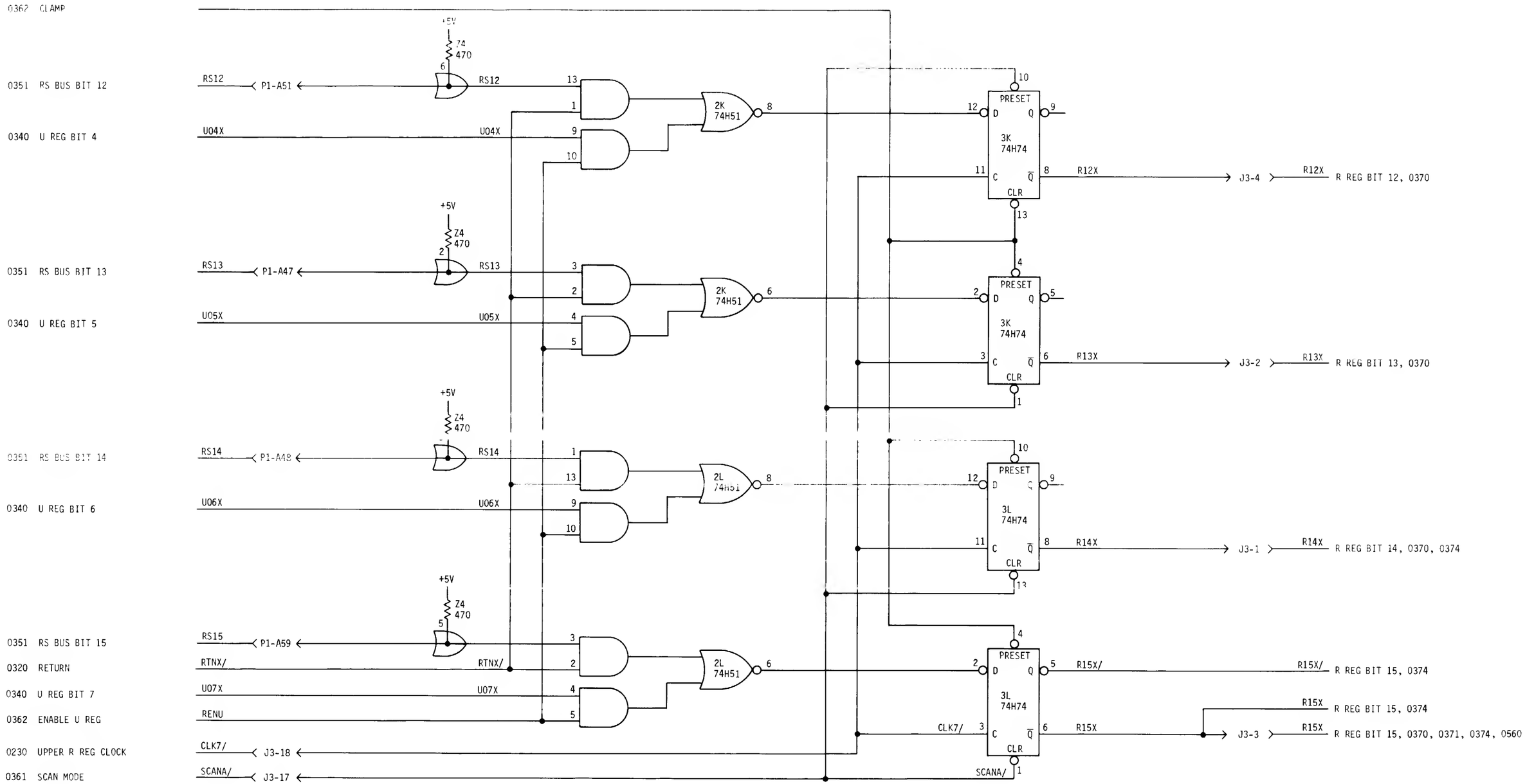
0351 RS BUS BIT 12

0351 RS BUS BIT 13

0351 RS BUS BIT 14

0350 RS BUS BIT 0
0350 RS BUS BIT 1
0350 RS BUS BIT 2
0351 RS BUS BIT 15





UPPER R REGISTER BITS 12-15

J3 DATA BOARD
0363

OP CODE DECODER

0363 R REG BIT 12
0363 R REG BIT 13
0363 R REG BIT 14
0363 R REG BIT 15

R12X ← J3-4 ← R12X 23 A0
R13X ← J3-2 ← R13X 22 A1
R14X ← J3-1 ← R14X 21 A2
R15X ← J3-3 ← R15X 20 A3

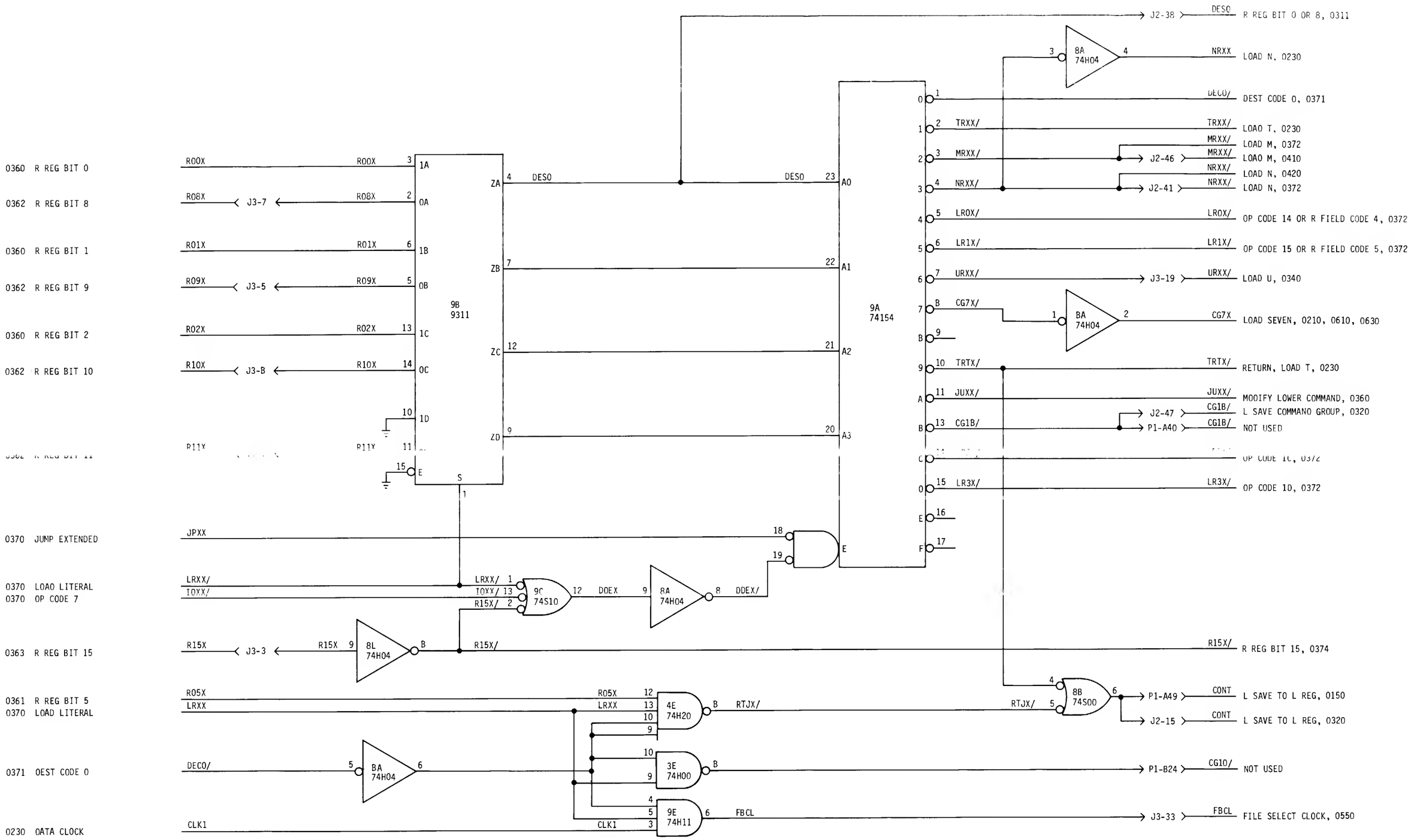
9L 74154

0 1 JPXX/
1 2 LRXX/
2 3 LFXX/
3 4 AFXX/
4 5 TZXX/
5 6 TNXX/
6 7 CPXX/
7 8 IOXX/
8 9 ADXX/
9 10 SBXX/
A 11 MYXX/
B 13 CYXX/
C 14 ORXX/
D 15 XRXX/
E 16 ANXX/
F 17 SHXX/

18, 19 → E

JPXX/ → P1-B27 → JPXX/ NOT USED
JPXX/ JUMP EXTENDED, 0372
J2-23 → JPXX/ JUMP EXTENDED, 0311, 0320, 0374
LRXX/ LOAD LITERAL, 0371, 0372
LFXX/ LOAD FILE, 0230, 0372
AFXX/ ADD FILE, 0230
TZXX/ TEST IF ZERO, 0211, 0372
TNXX/ TEST IF NOT ZERO, 0211, 0372
CPXX/ COMPARE FILE, 0560
IOXX/ OP CODE 7, 0371, 0372, 0570
J2-21 → IOXX/ OP CODE 7, 0374
ADXX/ ADD COMMAND, 0372, 0560
SBXX/ SUBTRACT COMMAND, 0372, 0374, 0560
J3-29 → SBXX/ SUBTRACT COMMAND, 0810
MYXX/ MEMORY READ OR WRITE, 0372, 0374, 0560, 0570
J2-25 → MYXX/ MEMORY READ OR WRITE, 0374
CYXX/ COPY, 0372
ORXX/ OR COMMAND, 0372
J3-11 → ORXX/ OR COMMAND, 0520
J3-10 → XRXX/ EXCLUSIVE OR COMMAND, 0520
ANXX/ AND WITH FILE, 0372
SHXX/ SHIFT FILE, 0560

JPXX/ 1 → 9K 74H04 → 2 JPXX → JPXX JUMP EXTENDED, 0371
LRXX/ 13 → 9K 74H04 → 12 → J3-35 → LRXX LOAD LITERAL, 0311
LRXX LOAD LITERAL, 0210, 0230, 0371, 0610, 0630
CPXX/ 11 → 9K 74H04 → 10 CPXX → CPXX COMPARE FILE, 0211
IOXX/ 5 → 8L 74H04 → 6 IOXX → IOXX OP CODE 7, 0372, 0373
SBXX/ 3 → 9K 74H04 → 4 SBXX → SBXX SUBTRACT COMMAND, 0374, 0560
MYXX/ 3 → 8L 74H04 → 4 MYXX → MYXX MEMORY READ OR WRITE, 0211, 0374, 0450, 0560
SHXX/ 5 → 9K 74H04 → 6 SHXX → J2-49 → SHXX SHIFT FILE, 0570
SHXX SHIFT FILE, 0372, 0373, 0560



DESTINATION DECODER

J2 CONTROL BOARD
0371

SECOND-LEVEL COMMAND DECODES

0211 RUN INHIBIT
0211 CLOCK STOP

RINH/
CSTP/

RINH/ 9
10
11
6B 74H10
8 LRLL/

J2-44 > LRLL/ LOAD L REG, 0310, 0311

0371 OP CODE 1D
0371 OP CODE 1C
0371 OP CODE 15 OR R FIELD CODE 5
0371 OP CODE 14 OR R FIELD CODE 4
0370 JUMP EXTENDED

LR3X/
LR2X/
LR1X/
LROX/
JPXX/

LR3X/ 12
11
LR2X/ 6
LR1X/ 5
4
LROX/ 3
JPXX/ 2
1
7A 74H20
8 LRO1

13 8A 74H04 12 > LRO1/ JUMP, 0211, 0230

LRO1 JUMP, 0210

0370 LOAD FILE
0370 LOAD LITERAL
0370 COPY

LFXX/
LRXX/
CYXX/

13
LFXX/ 12
LRXX/ 10
CYXX/ 9
9J 74H20
8 FINH

J3-45 > FINH FILE INHIBIT, 0550

0361 R REG BIT 5
0370 OP CODE 7

RO5X/
IOXX/

RO5X/ 4
IOXX/ 5
2H 7437
6

J3-28 > IDHT SEL UNCOMP INPUT DATA, 0810

0370 SHIFT FILE

SHXX

RO5X/ 9
SHXX 10
5K 74H00
8 SHLX/

9 6L 74H04 8 > SHLX SHIFT LEFT, 0560

J3-12 > SHLX/ SHIFT LEFT, 0520

0374 OP CODE C, D, E OR F
0370 OR COMMAND

LSGX/
ORXX/

IOXX/ 1
LSGX/ 2
ORXX/ 12
13
8J 74H30
8

11 8L 74H04 10 > J2-48 > ADOX OP CODES 0-3, 6, 8-B, 05/0

0370 AND WITH FILE
0370 TEST IF NOT ZERO
0370 TEST IF ZERO

ANXX/
TNXX/
TZXX/

EXIO 6
ANXX/ 3
TNXX/ 4
TZXX/ 5

4
5
2
1
9J 74H20
6

9 9K 74H04 8 > J3-21 > ANDX/ LOGICAL AND, 0520

0370 OP CODE 7
0361 R REG BIT 7

IOXX
RO7X

5
8K 74S00
4
6 EXIO

J2-37 > EXIO EXTERNAL I/O COMMAND, 0810

+5V
R53 470

0370 ADD COMMAND
0370 SUBTRACT COMMAND
0370 MEMORY READ OR WRITE
0370 COPY

ADXX/
SBXX/
MYXX/
CYXX/

ADXX/ 1
SBXX/ 4
MYXX/ 5
CYXX/ 2
7J 74H22
6

9 7H 74H04 8 > J2-7 > TONY/ OP CODES 8-B, 0374

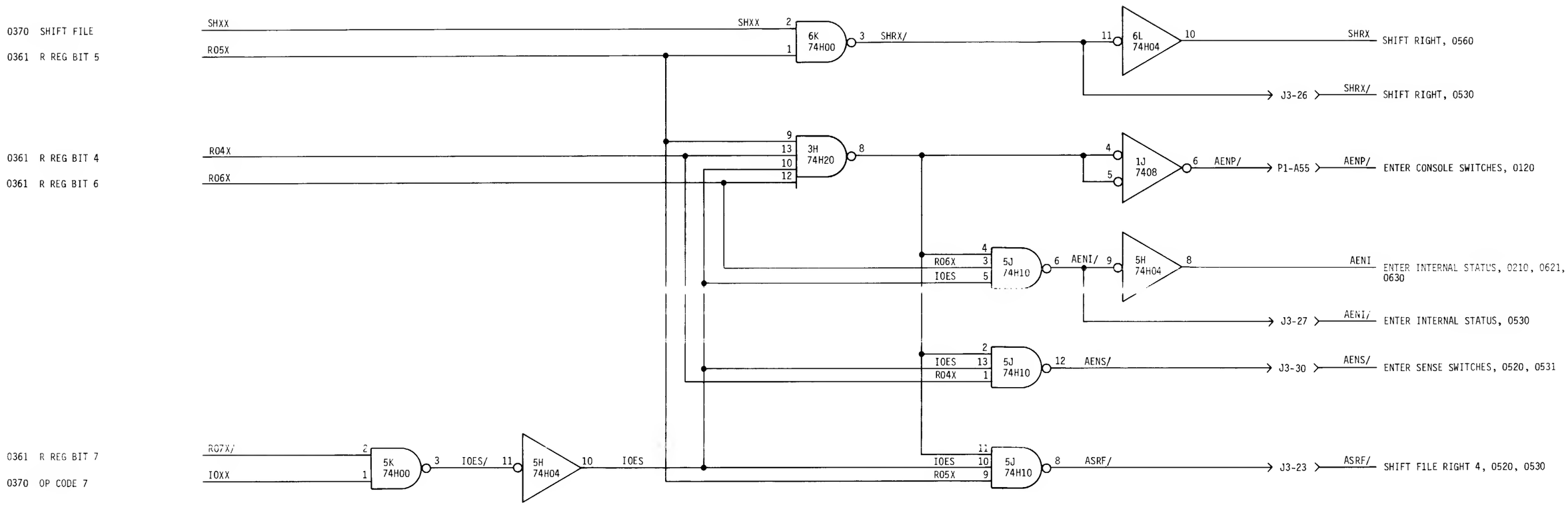
0371 LOAD N
0371 LOAD M

NRXX/
MRXX/

NRXX/ 2
MRXX/ 1
8B 74S00
3 MNRX

11 8A 74H04 10 > MNRX/ M OR N REG SELECT, 0560

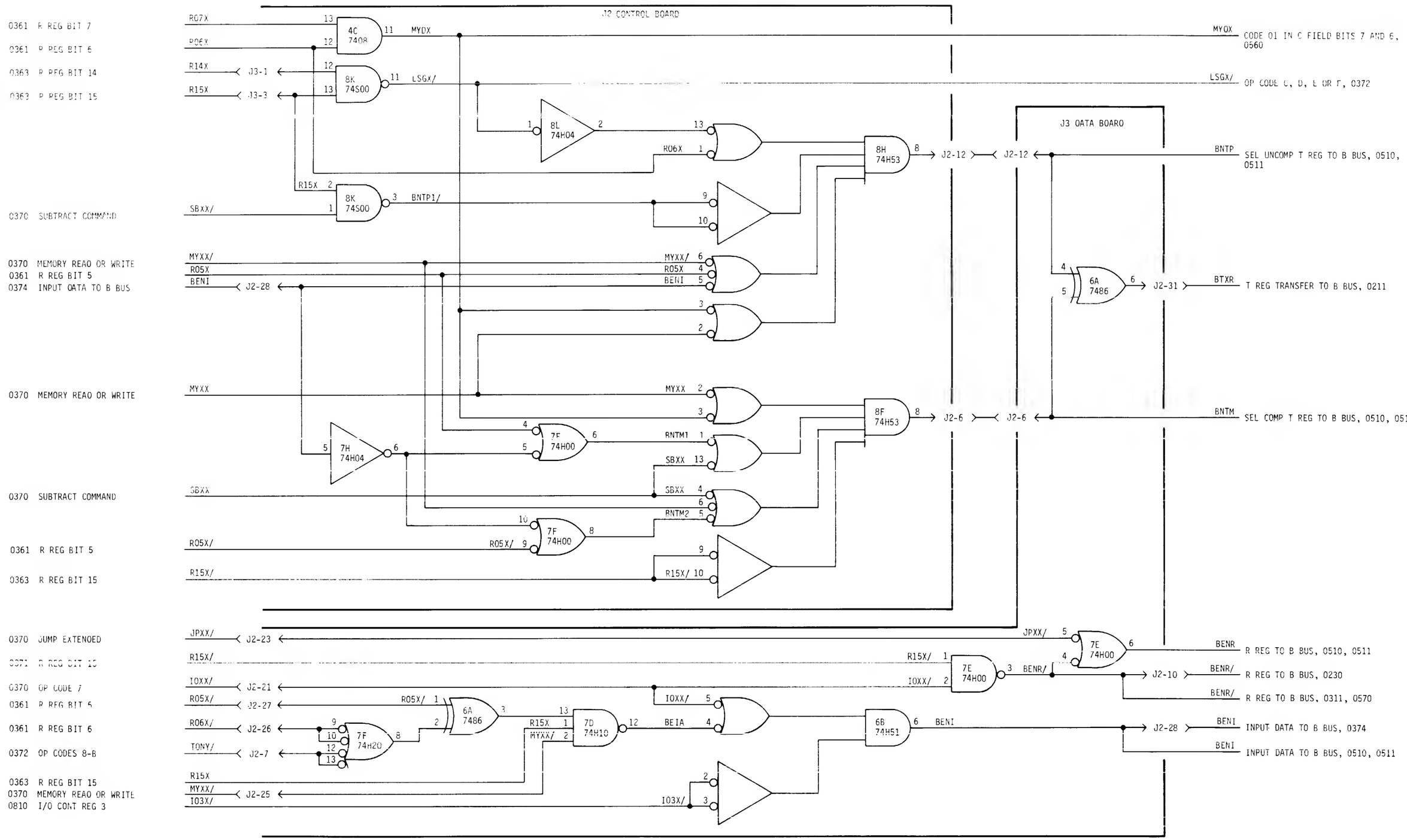
MNRX M OR N REG SELECT, 0211, 0560

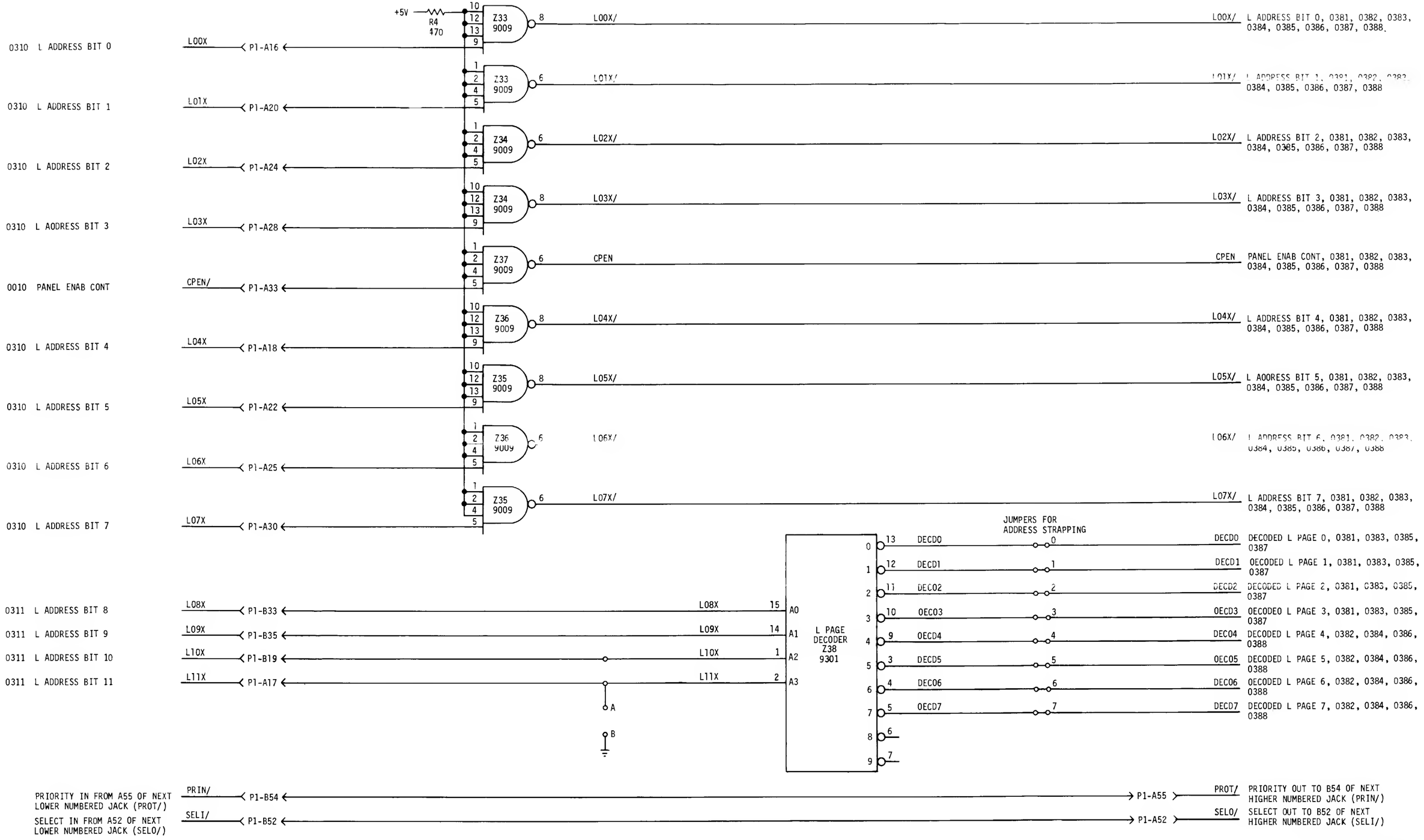


A BUS DATA SELECT DECODES

J2 CONTROL BOARD
0373

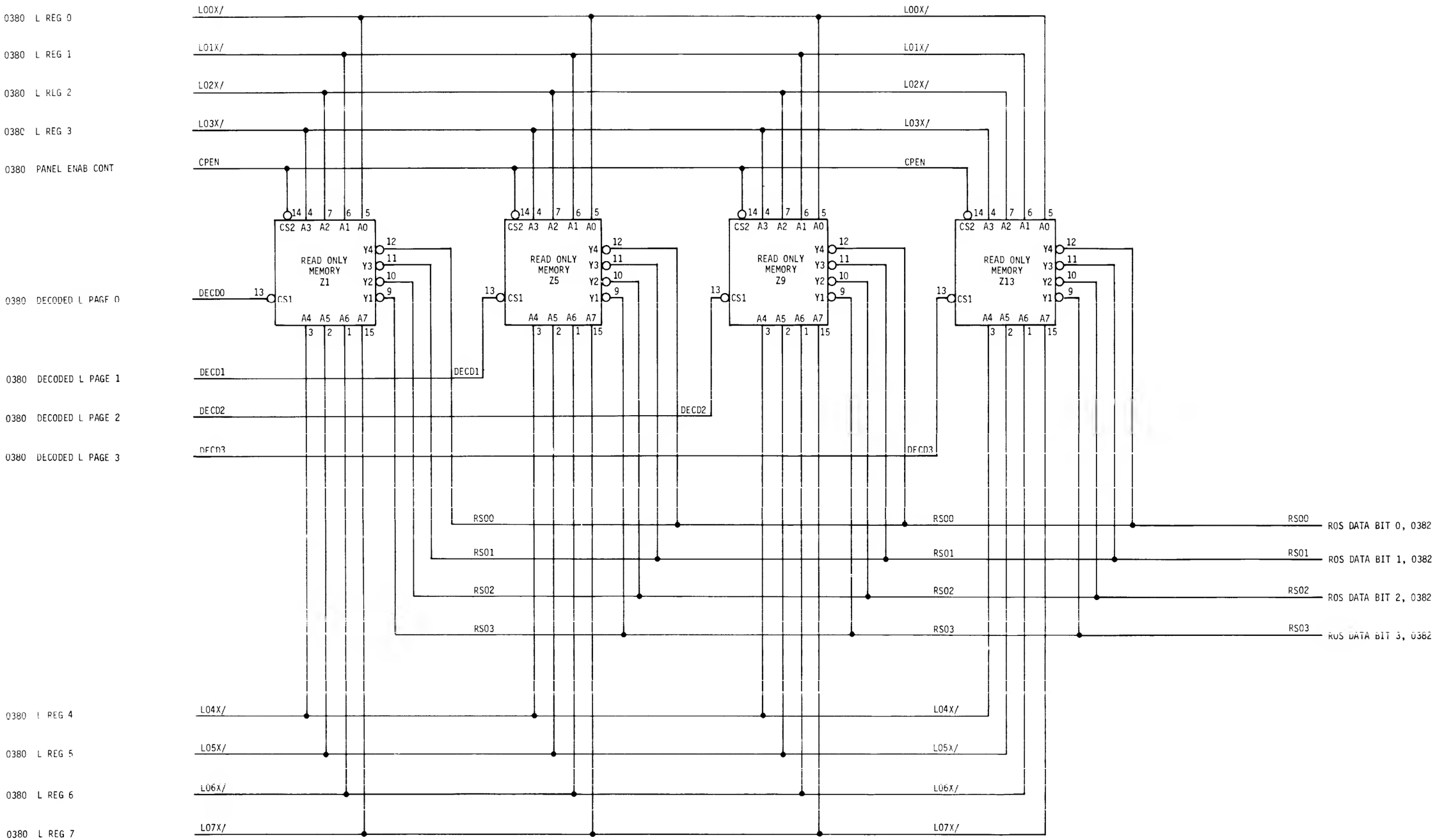
B BUS DATA SELECT DECODES

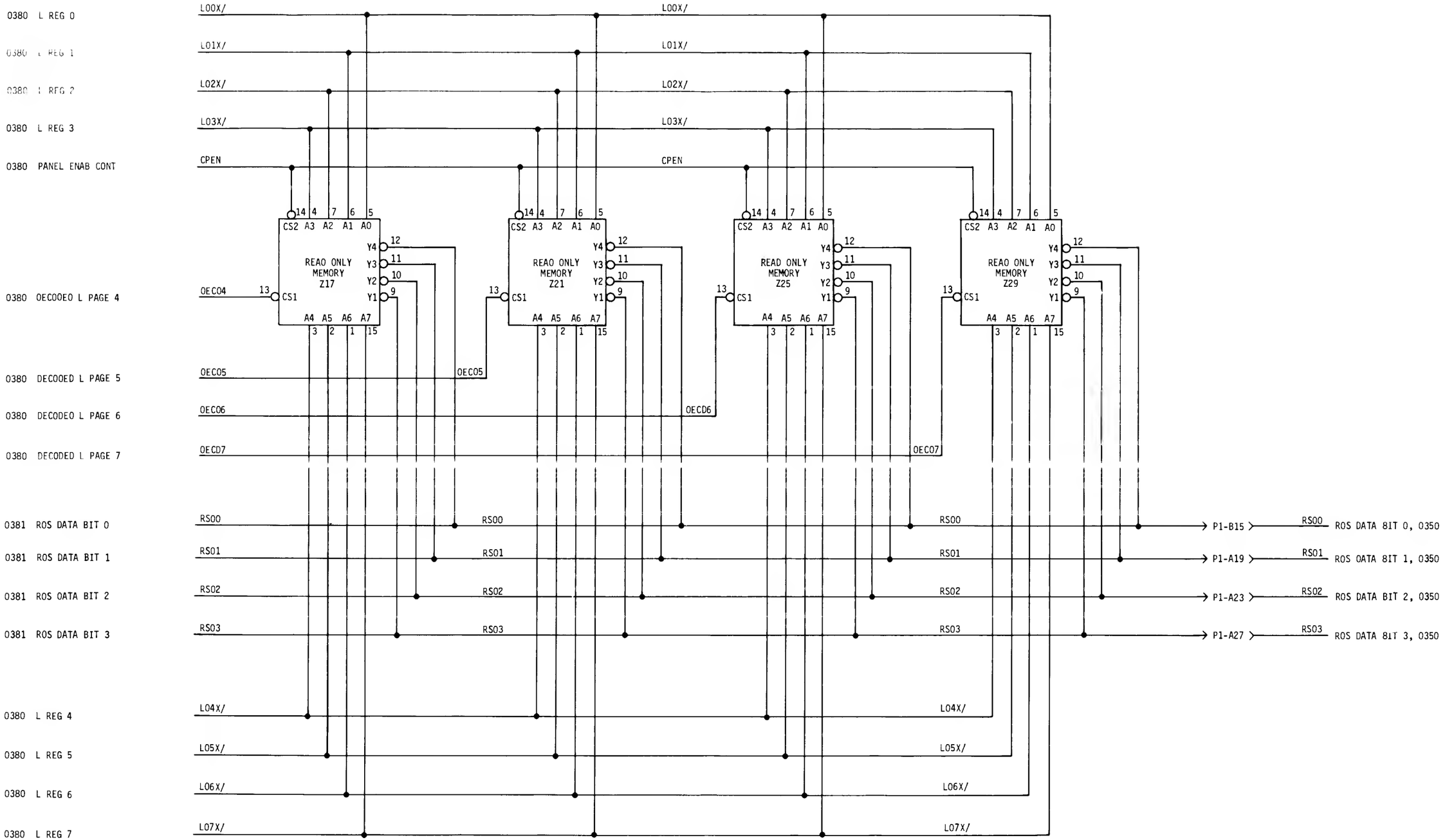




READ ONLY MEMORY CONTROL

READ ONLY MEMORY BOARD
0380


0380 L REG 0
0380 L REG 1
0380 L RLG 2
0380 L REG 3
0380 PANEL ENAB CONT
0380 DECODED L PAGE 0
0380 DECODED L PAGE 1
0380 DECODED L PAGE 2
0380 DECODED L PAGE 3
0380 L REG 4
0380 L REG 5
0380 L REG 6
0380 L REG 7
L00X/
L01X/
L02X/
L03X/
CPEN
L04X/
L05X/
L06X/
L07X/
DECD0
DECD1
DECD2
DECD3
RS00
RS01
RS02
RS03
READ ONLY MEMORY Z1
READ ONLY MEMORY Z5
READ ONLY MEMORY Z9
READ ONLY MEMORY Z13
CS2 A3 A2 A1 A0
A4 A5 A6 A7
CS1
Y4 Y3 Y2 Y1
ROS DATA BIT 0, 0382
ROS DATA BIT 1, 0382
ROS DATA BIT 2, 0382
ROS DATA BIT 3, 0382

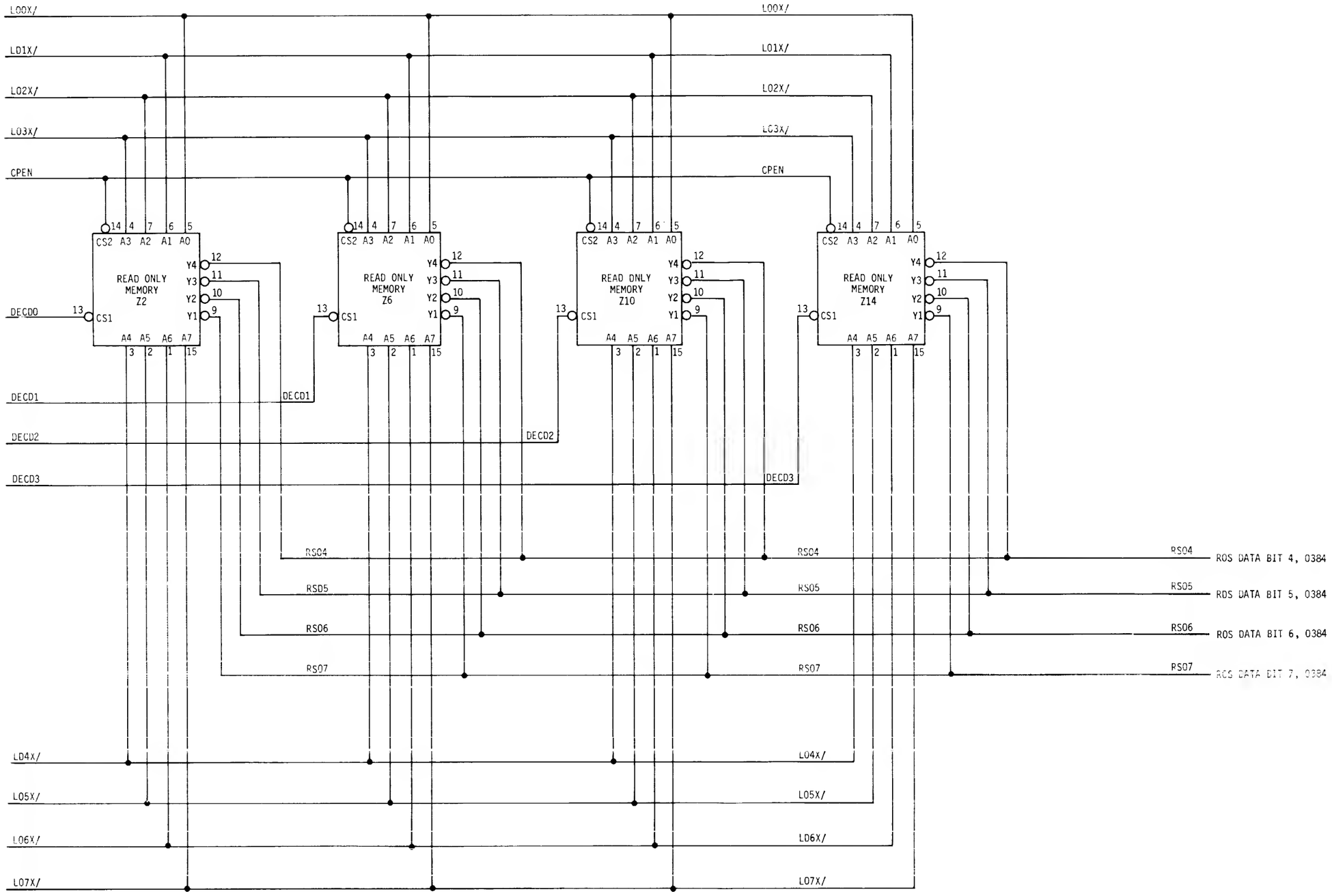


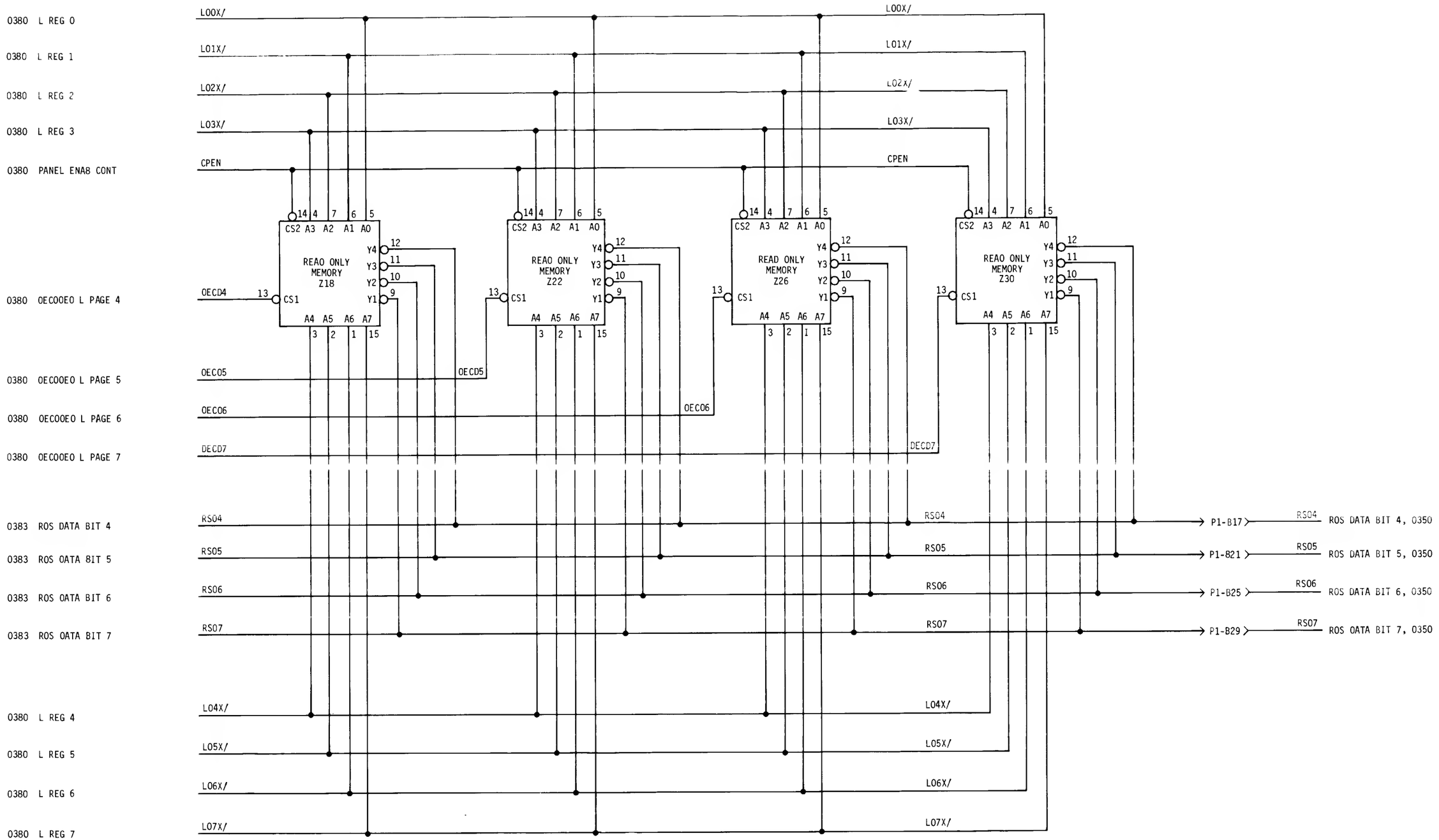
READ ONLY MEMORY BITS 17, 21, 25, 29

READ ONLY MEMORY BOARD
0382

READ ONLY MEMORY BITS 2, 6, 10, 14

0380 L REG 0
0380 L REG 1
0380 L REG 2
0380 L REG 3
0380 PANEL ENAB CONT
0380 DECODED L PAGE 0
0380 DECODED L PAGE 1
0380 DECODED L PAGE 2
0380 DECODED L PAGE 3
0380 L REG 4
0380 L REG 5
0380 L REG 6
0380 L REG 7

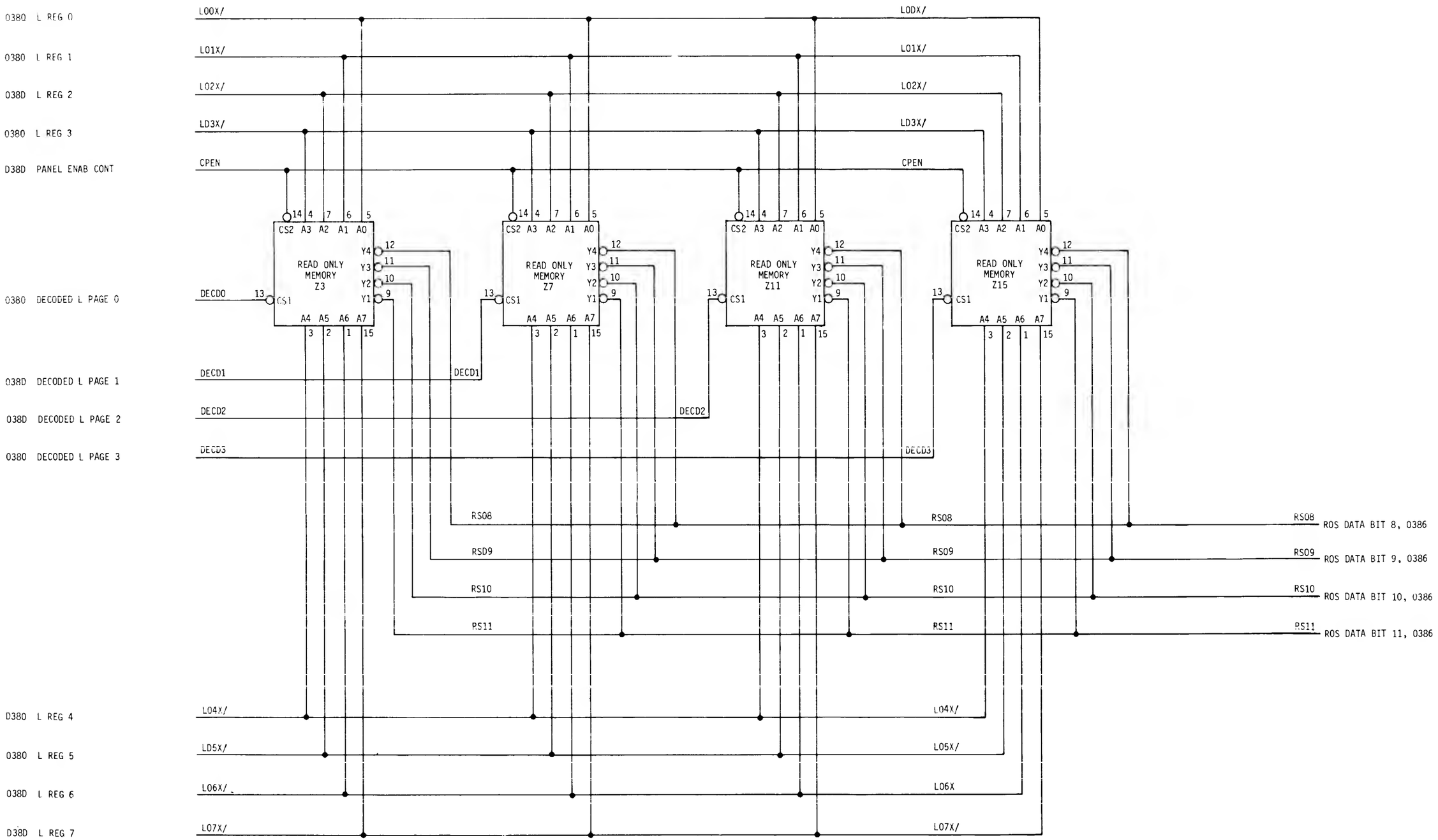


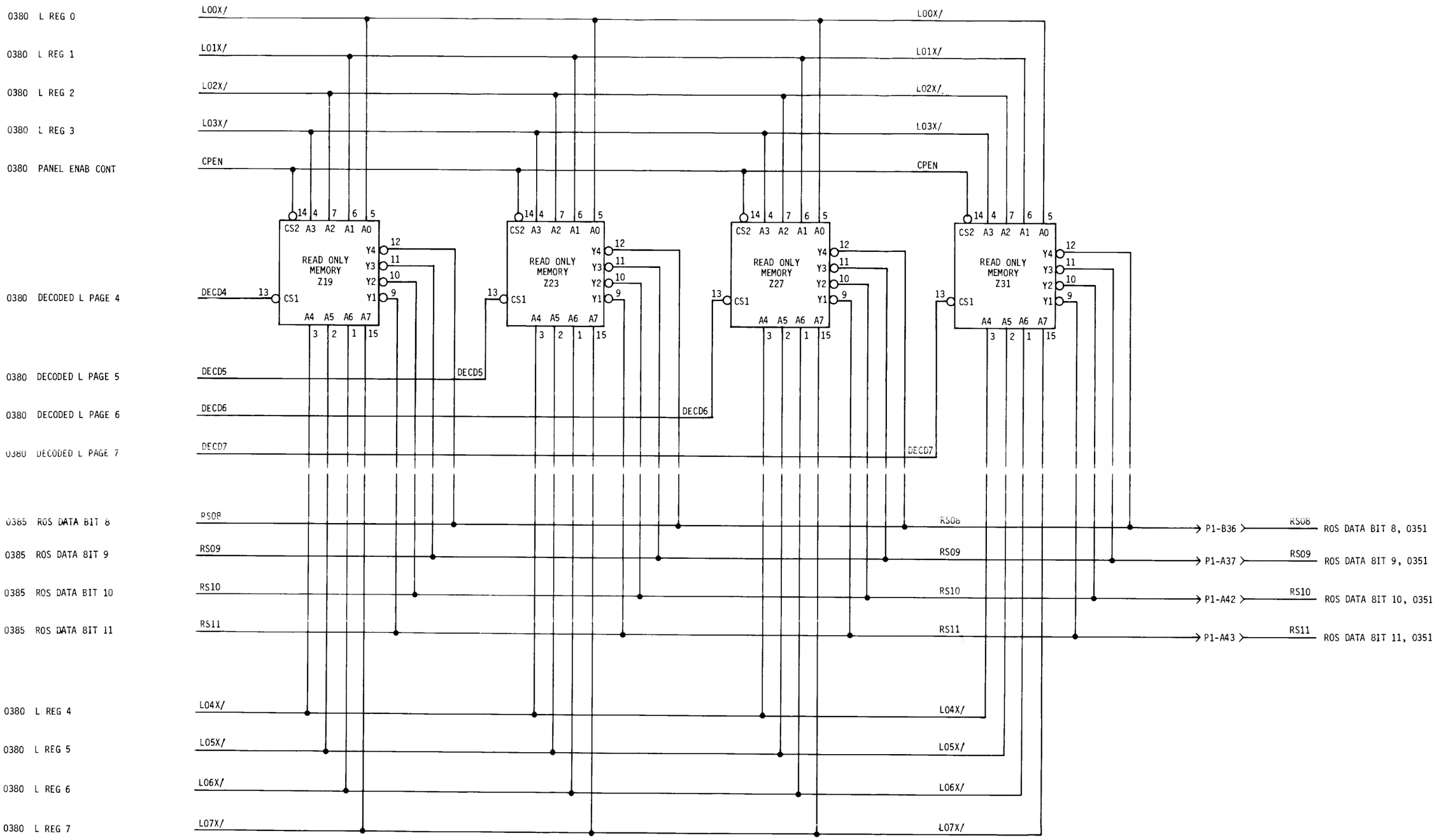


READ ONLY MEMORY BITS 18, 22, 26, 30

READ ONLY MEMORY BOARD
0384

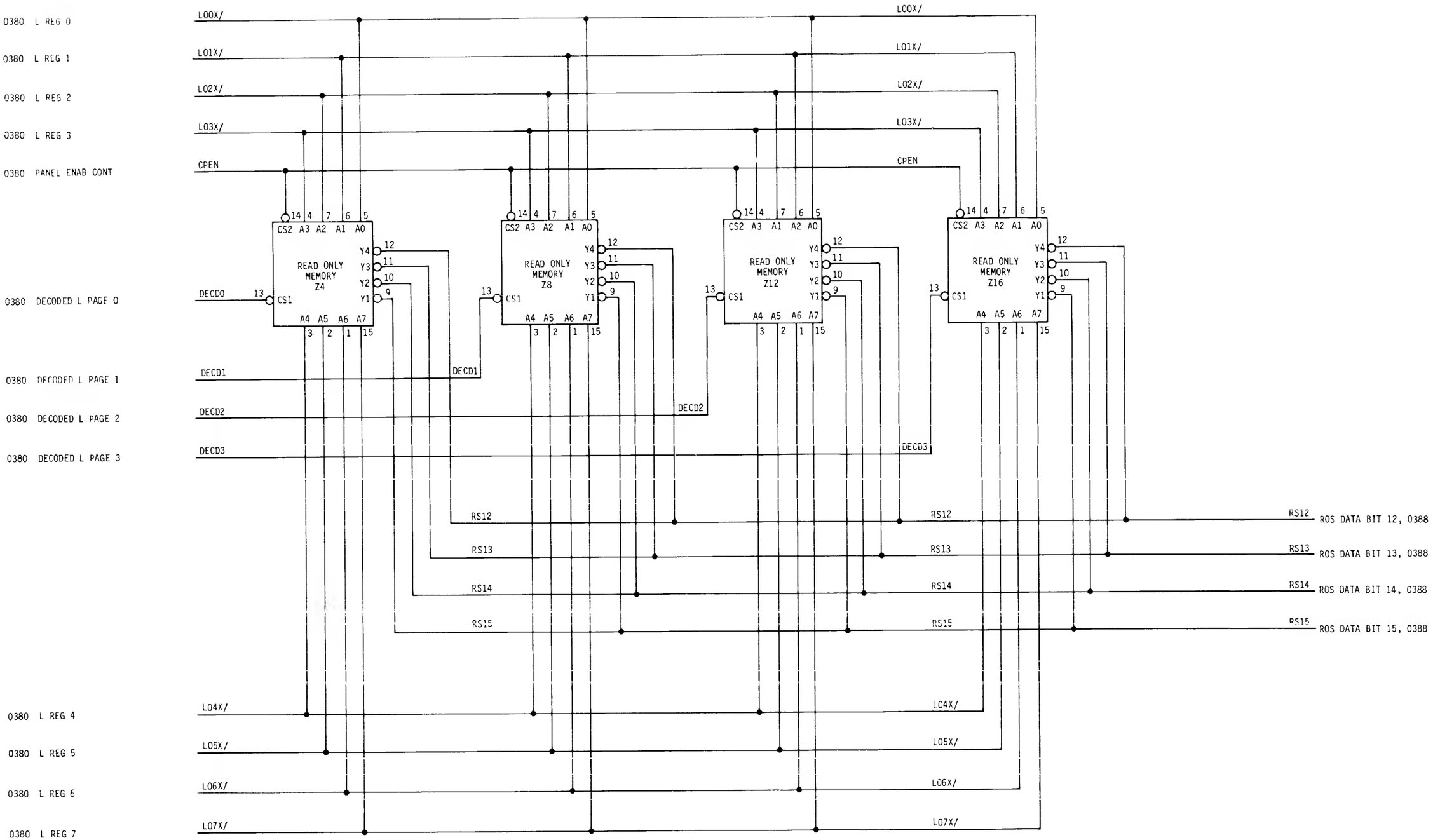
READ ONLY MEMORY BITS 3, 7, 11, 15

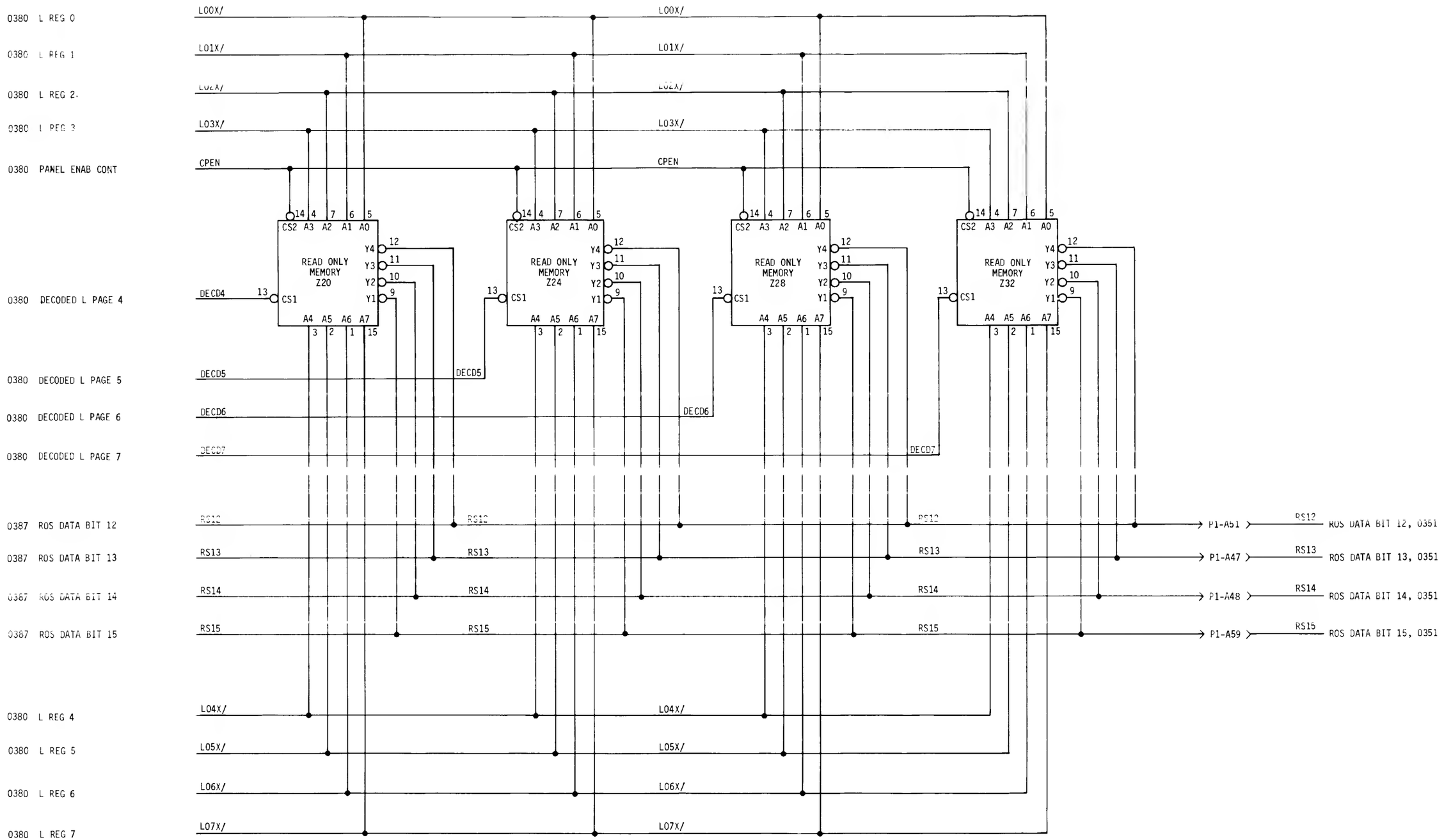




READ ONLY MEMORY BITS 19, 23, 27, 31

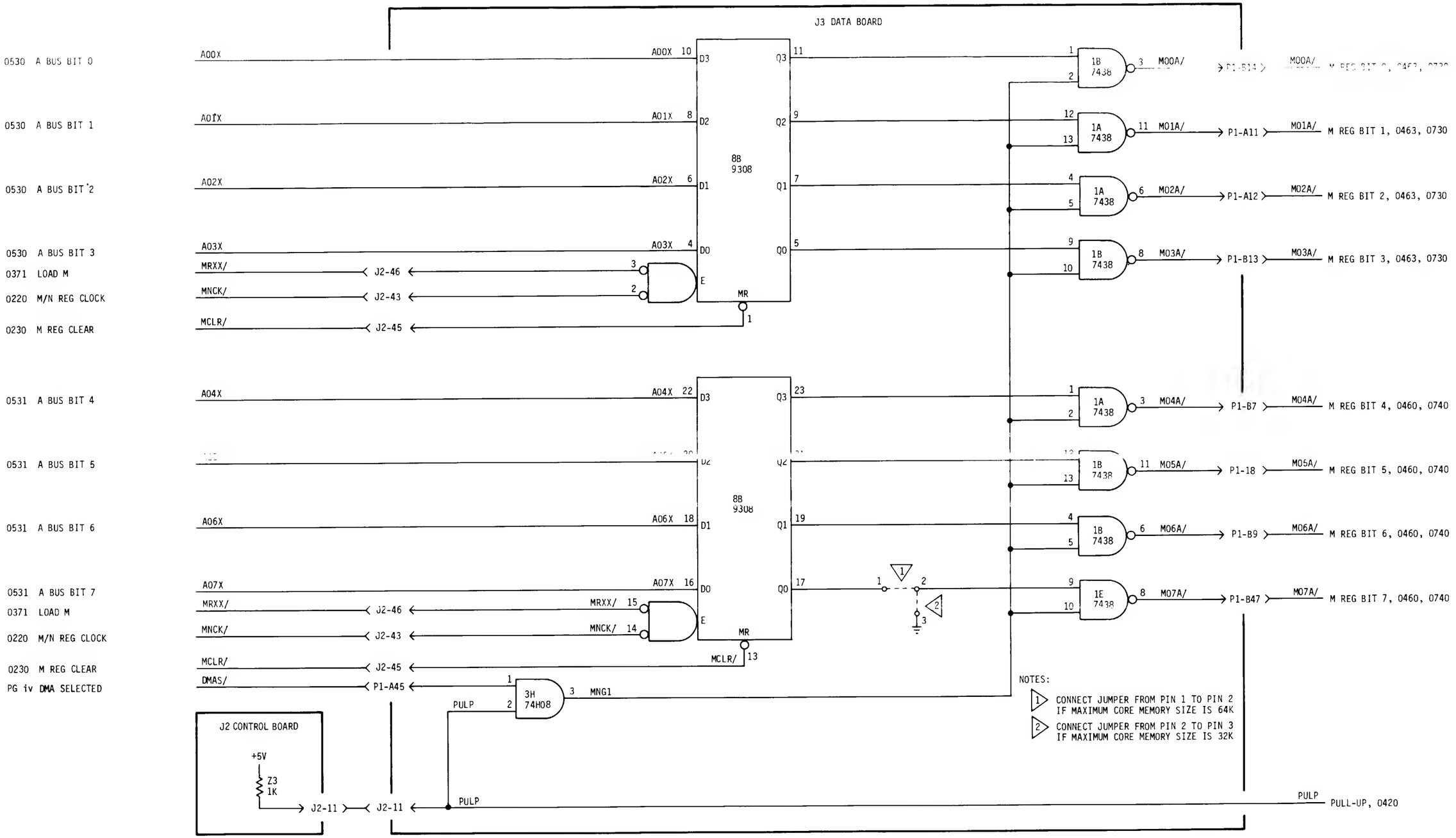
READ ONLY MEMORY BOARD
0386


0380 L REG 0
0380 L REG 1
0380 L REG 2
0380 L REG 3
0380 PANEL ENAB CONT
0380 DECODED L PAGE 0
0380 DECODED L PAGE 1
0380 DECODED L PAGE 2
0380 DECODED L PAGE 3
0380 L REG 4
0380 L REG 5
0380 L REG 6
0380 L REG 7
L00X/
L01X/
L02X/
L03X/
CPEN
L04X/
L05X/
L06X/
L07X/
DECD0
DECD1
DECD2
DECD3
READ ONLY MEMORY Z4
READ ONLY MEMORY Z8
READ ONLY MEMORY Z12
READ ONLY MEMORY Z16
CS2 A3 A2 A1 A0
CS1
A4 A5 A6 A7
Y4 Y3 Y2 Y1
RS12
RS13
RS14
RS15
ROS DATA BIT 12, 0388
ROS DATA BIT 13, 0388
ROS DATA BIT 14, 0388
ROS DATA BIT 15, 0388



READ ONLY MEMORY BITS 20, 24, 28, 32

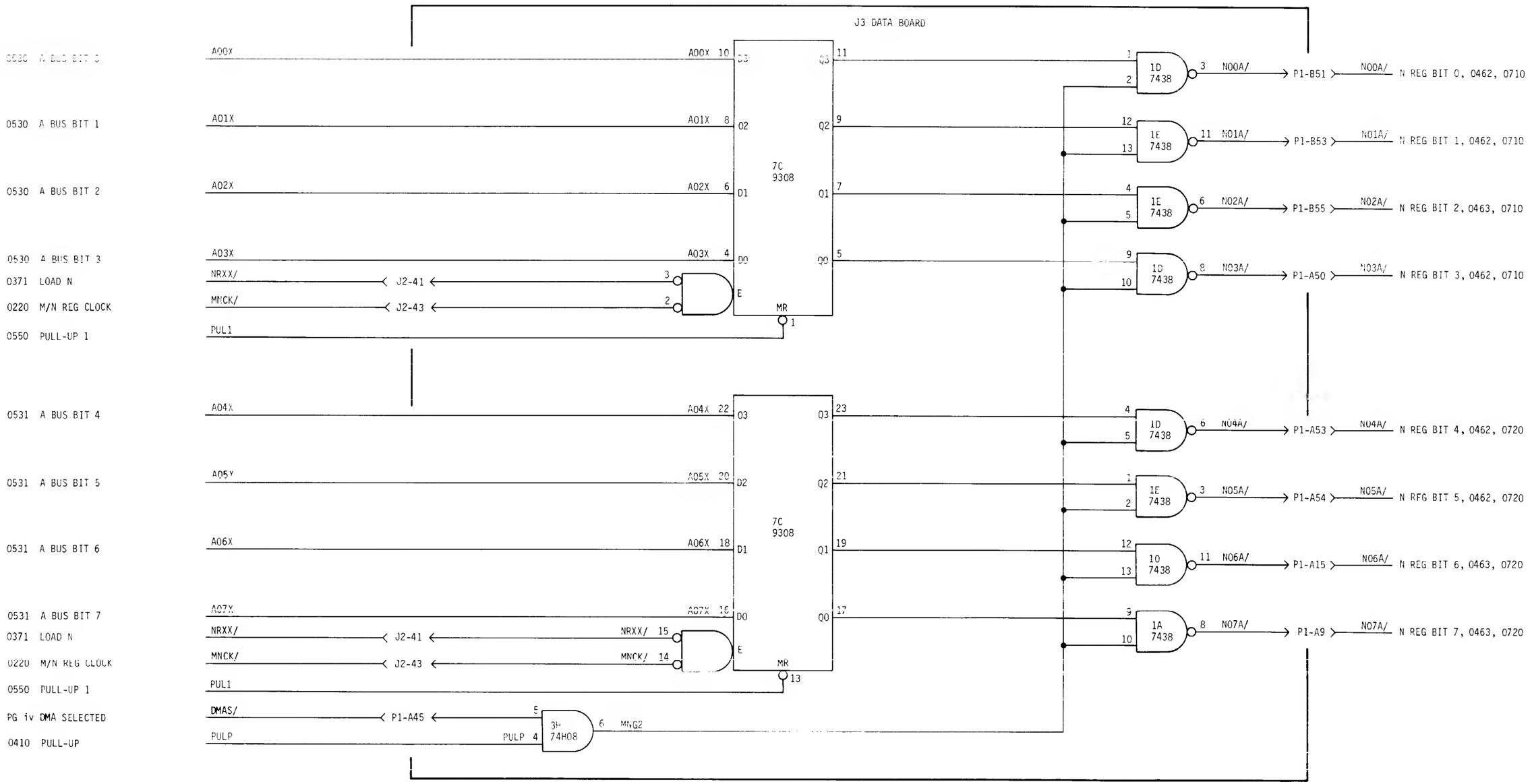
READ ONLY MEMORY BOARD
0388

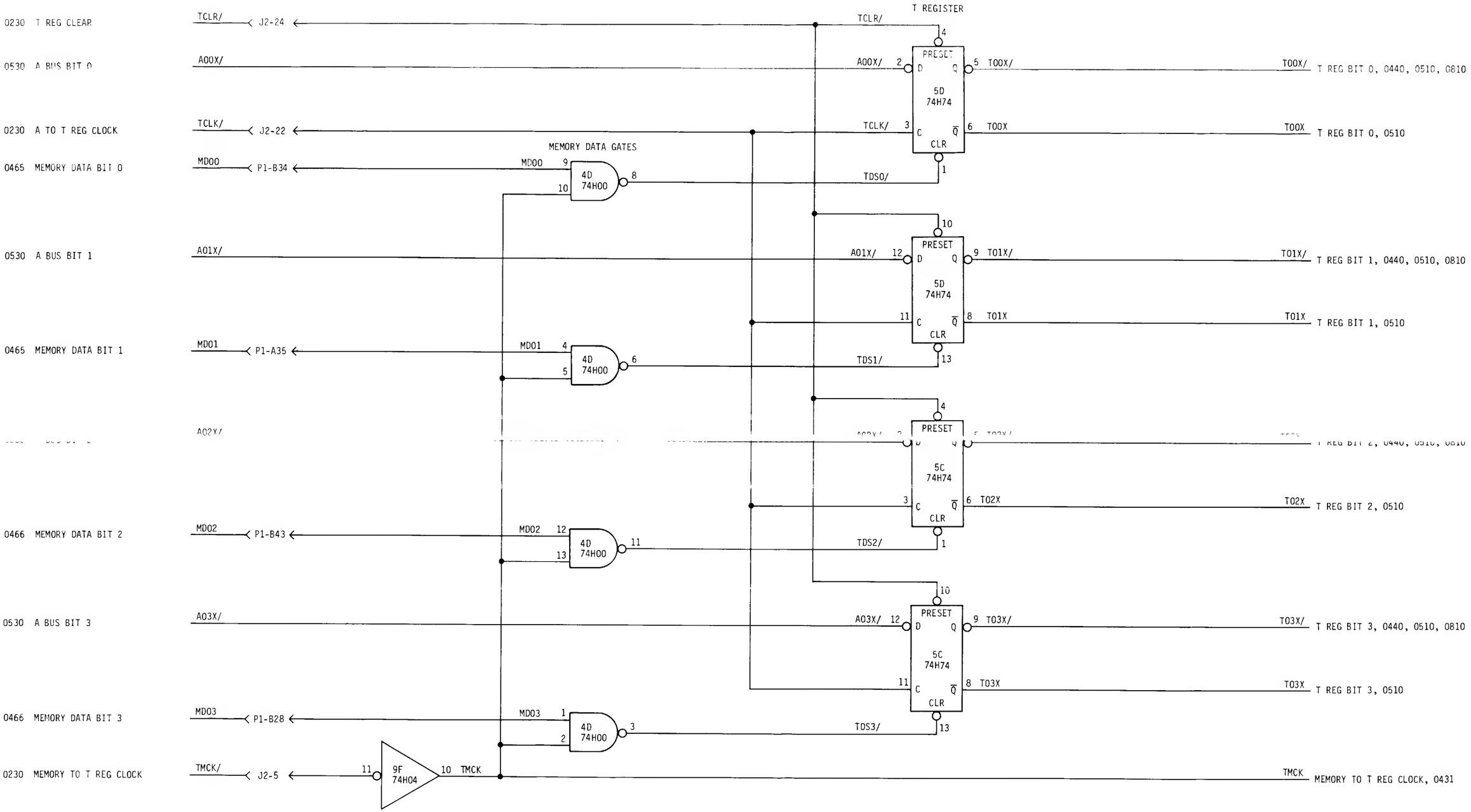


M REGISTER

J2 CONTROL BOARD
AND J3 DATA BOARD
0410

N REGISTER

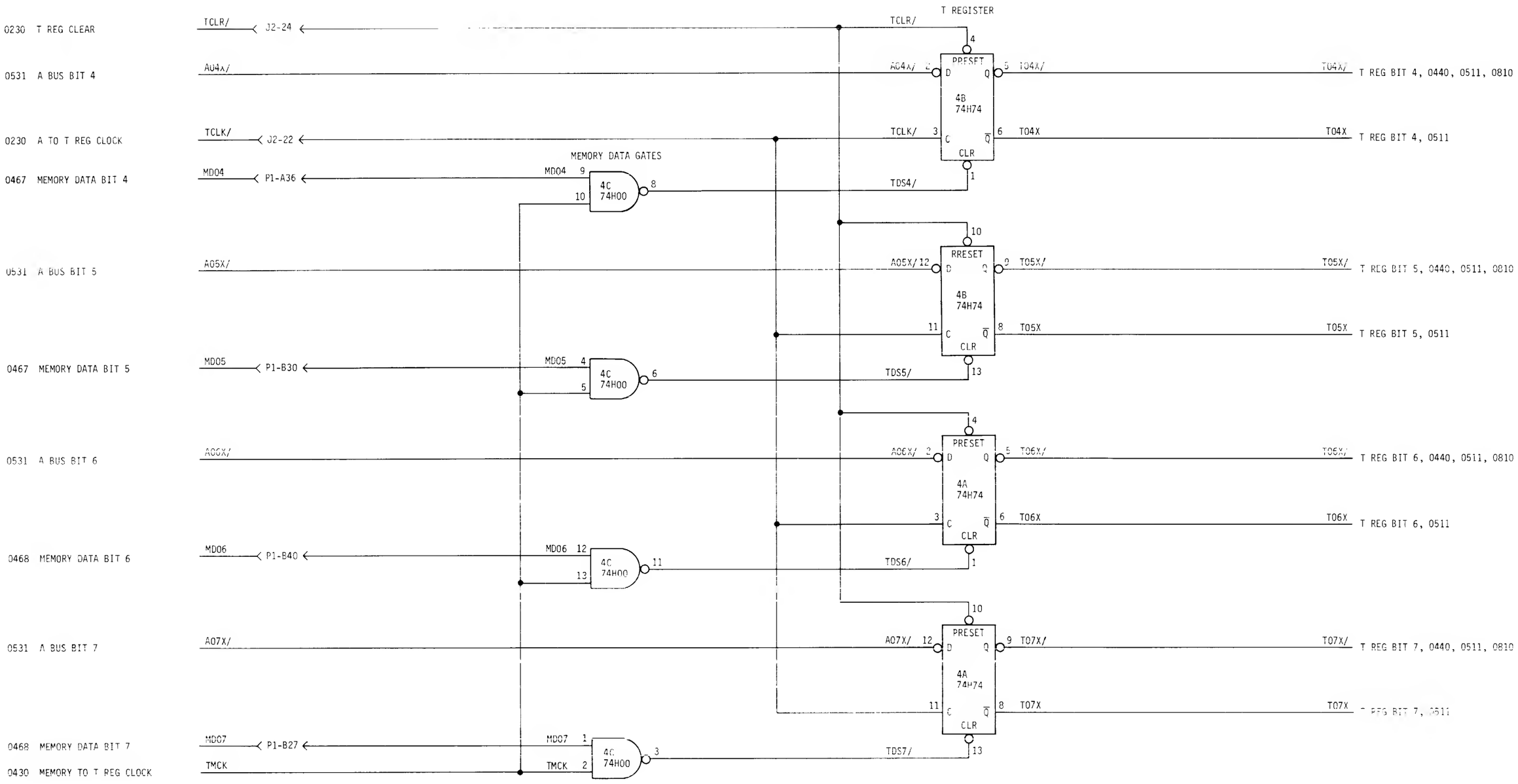

J3 DATA BOARD
0530 A BUS BIT 0
0530 A BUS BIT 1
0530 A BUS BIT 2
0530 A BUS BIT 3
0371 LOAD N
0220 M/N REG CLOCK
0550 PULL-UP 1
0531 A BUS BIT 4
0531 A BUS BIT 5
0531 A BUS BIT 6
0531 A BUS BIT 7
0371 LOAD N
0220 M/N REG CLOCK
0550 PULL-UP 1
PG iv DMA SELECTED
0410 PULL-UP
A00X
A01X
A02X
A03X
A04X
A05X
A06X
A07X
NRXX/
MNCK/
PUL1
DMAS/
PULP
J2-41
J2-43
P1-A45
7C 9308
3H 74H08
1D 7438
1E 7438
1A 7438
1C 7438
N00A/
N01A/
N02A/
N03A/
N04A/
N05A/
N06A/
N07A/
P1-B51
P1-B53
P1-B55
P1-A50
P1-A53
P1-A54
P1-A15
P1-A9
N REG BIT 0, 0462, 0710
N REG BIT 1, 0462, 0710
N REG BIT 2, 0463, 0710
N REG BIT 3, 0462, 0710
N REG BIT 4, 0462, 0720
N RFG BIT 5, 0462, 0720
N REG BIT 6, 0463, 0720
N REG BIT 7, 0463, 0720
MR
MNG2

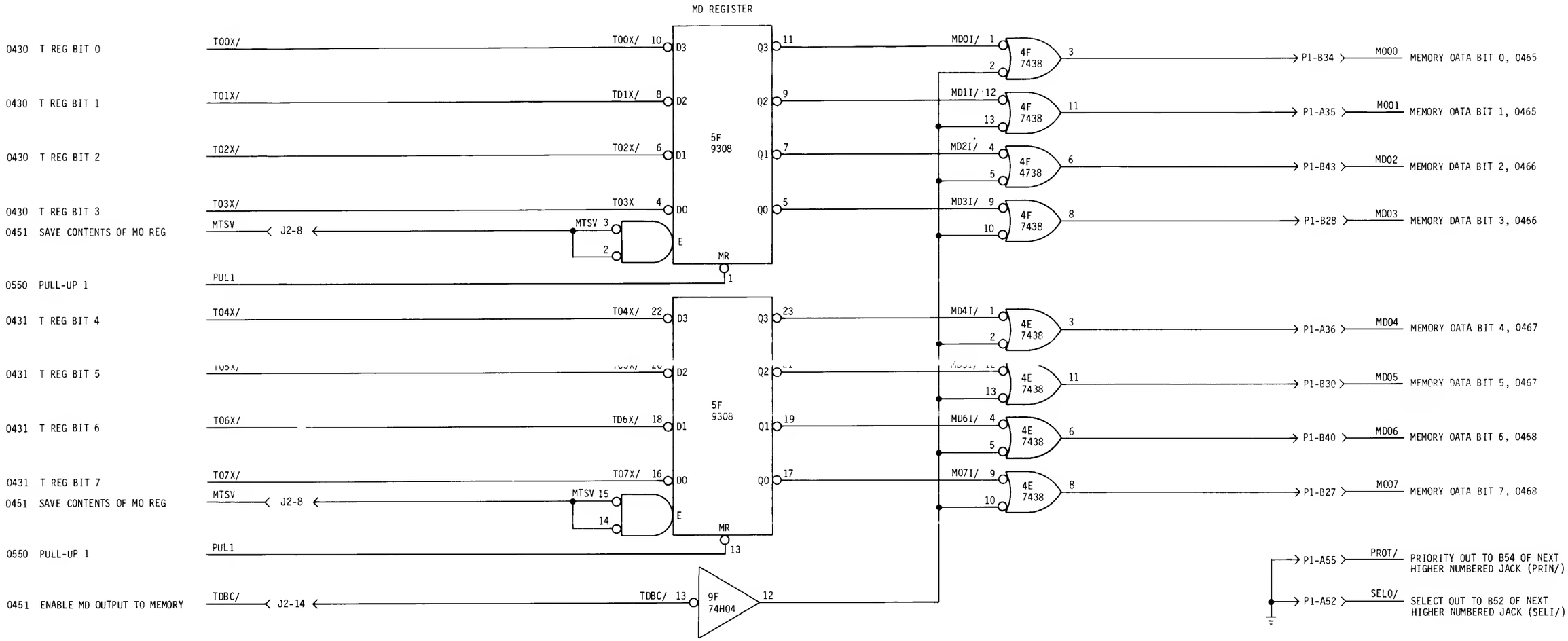


MEMORY DATA GATES AND T REGISTER BITS 0-3

J3 DATA BOARD
0430

MEMORY DATA GATES AND T REGISTER BITS 4-7





MEMORY DATA (MD) REGISTER, PRIORITY/SELECT

J3 DATA BOARD
0440

PG iv MASTER RESET

0220 MEMORY CLOCK PHASE 1
0220 MEMORY CLOCK PHASE 2
0451 WRITE INHIBIT 0 S

0451 WRITE PULSE INTERNAL
0361 R REG BIT 4

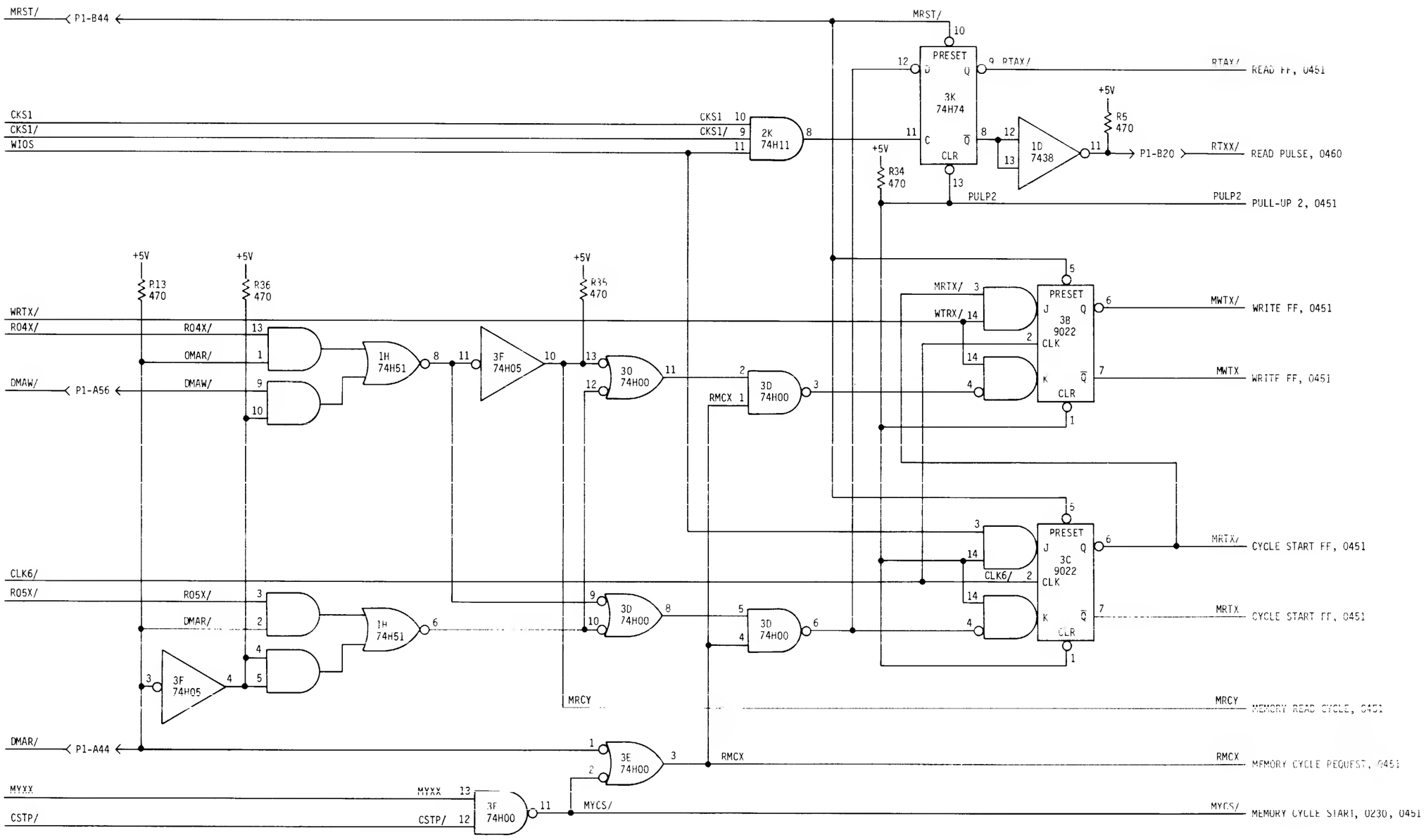
PG iv DMA WRITE

0230 5-MHZ CLOCK PHASE 2
0361 R REG BIT 5

PG iv DMA REQUEST

0370 MEMORY READ OR WRITE

0211 CLOCK STOP



0450 WRITE FF

0450 CYCLE START FF

PG iv MASTER RESET

0450 PULL-UP 2

0230 5-MHZ CLOCK PULSE

0450 MEMORY CYCLE REQUEST

0450 MEMORY READ CYCLE

0450 MEMORY CYCLE START

0220 5-MHZ CLOCK PHASE 1

0451 WRITE PULSE 1NTERNAL

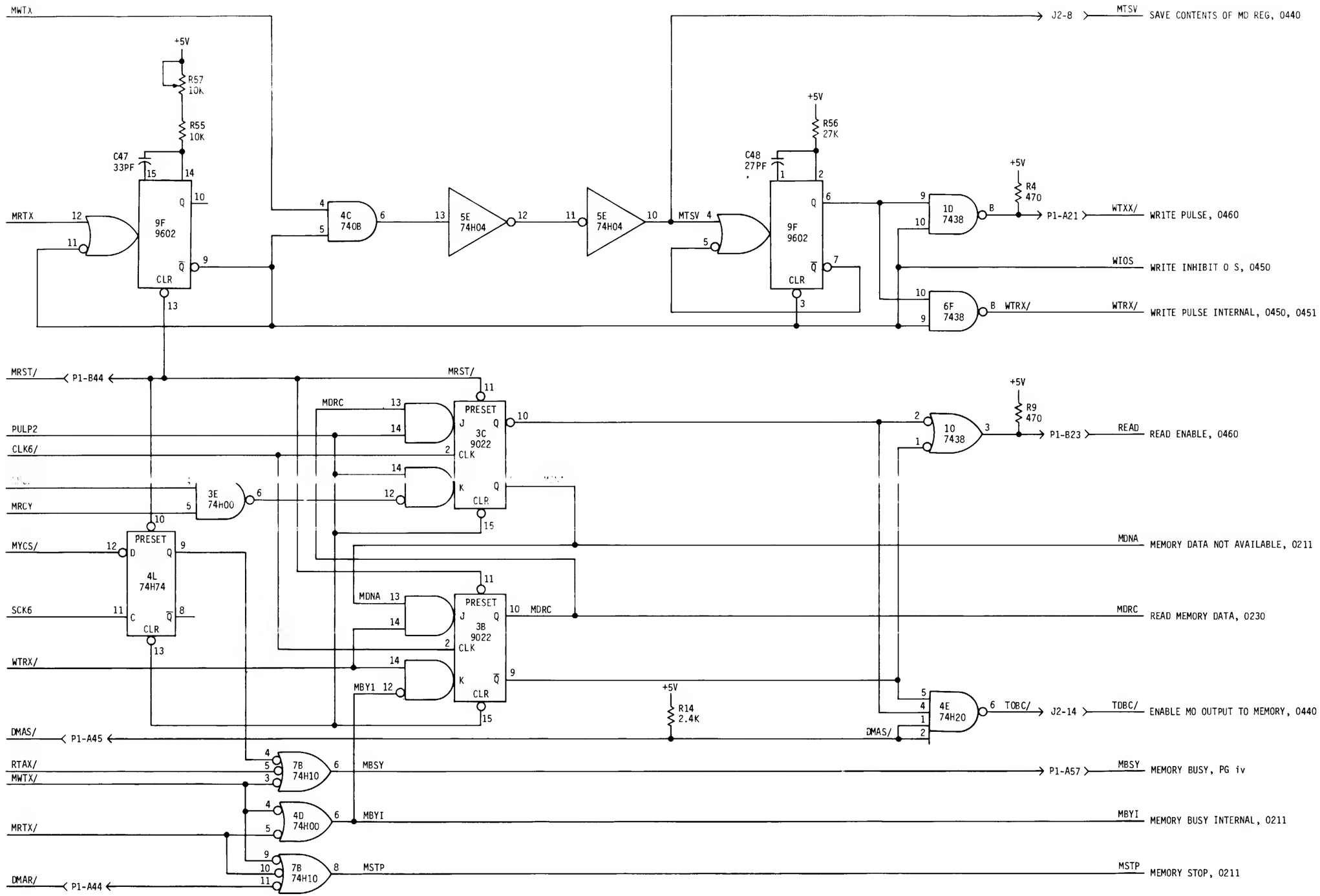
PG iv DMA SELECTEO

0450 READ FF

0450 WRITE FF

0450 CYCLE START FF

PG iv DMA REQUEST



MEMORY CONTROL 2

J2 CONTROL BOARD
0451

PG iv MASTER RESET

0450 READ PULSE

0410 M REG BIT 7

3 MEMORY SELECT 3

0410 M REG BIT 6

PG iv M REG BIT 6

3 MEMORY SELECT 2

0410 M REG BIT 5

PG iv M REG BIT 5

3 MEMORY SELECT 1

0451 WRITE PULSE

NOTES:

1. R2 AND R16 SELECTED FOR 345 nSEC OUTPUT AT PIN 7 OR 9.
2. C10 MAY BE ADDED IN TEST.
3. PINS B12, B16, and B45 ARE CONNECTED AS SHOWN IN THE CHART BELOW

MEMORY SIZE		8K	16K	24K	32K	40K	48K	56K	64K
	SLOT	J4	J5	J6	J7	J8	J9	J10	J11
SIGNAL	PIN								
MS1	B12	N/C	GRD	N/C	GRD	N/C	GRD	N/C	GRD
MS2	B16	N/C	N/C	GRD	GRD	N/C	N/C	GRD	GRD
MS3	B45	N/C	N/C	N/C	N/C	GRD	GRD	GRD	GRD

MRST/ P1-B44

RTXX/ P1-B20

MO7A/ P1-B47

MS3 P1-B45

MO6A/ P1-B9

MO6A/

MS2 P1-B16

MO5A/ P1-B18

MO5A/

MS1 P1-B12

WTXX/ P1-A21

YRXX/

+5V

R142 1K, R144 1K, R145 470, R146 4.7K

Z6 8242

Z4 74H11

MOS

MEN

C4 100pf, R1 10K, R2

Z2 9602 — 345 nSEC

YRXX

C5 100pf, R15 10K, R16

WTXX/

YWXX

C9 47pf, R39 10K

Z1 9602 — ≈ 200 nSEC

6 MCLR

MCLR/

MCLR

C10, R40 4.7K

Z1 9602 — 50-70 nSEC

RAS

RAS/

R47 10K

MRST/ → Z7 74H11 → EDEC/ ENABLE DECODER, 0462, 0463, 0540

YRXX/ → Z7 74411

YWXX/

MEN → Z7 74H11 → DCTO/ DRIVE CURRENT TURN-OFF, 0461

YRXX/ Y READ PULSE, 0461

YWXX/ Y WRITE PULSE, 0461

YWXX

Z5 9322 (I0a, I0b, I1b, I0c, I1c, I0d, I1d, E; Za, Zb, Zc, Zd)

7a ŌROW/ → ŌROW/ X READ/WRITE PULSE, 0461

Zb ŌROW/ → ŌROW/ X READ/WRITE PULSE, 0461

Zc ŌRAS → ŌRAS READ AMP STROBE UPPER STACK, 0465, 0466, 0467, 0468

Zd ORAS → ORAS READ AMP STROBE LOWER STACK, 0465, 0466, 0467, 0468

YWXX → Z3 9016 → ICTO INHIBIT CURRENT TURN-OFF, 0464

MLCR/ MEMORY LATCH CLEAR, 0465, 0466, 0467, 0468

MO4A → Z3 9016

YWXX, MEN → Z4 74H11 → Ō.WT WRITE LOWER STACK, 0465, 0466, 0467, 0468

MO4A, YWXX → Z4 74H11 → O.WT WRITE UPPER STACK, 0465, 0466, 0467, 0468

0410 M REG BIT 4

PG iv M REG BIT 4

MO4A/ → P1-B7

MO4A/

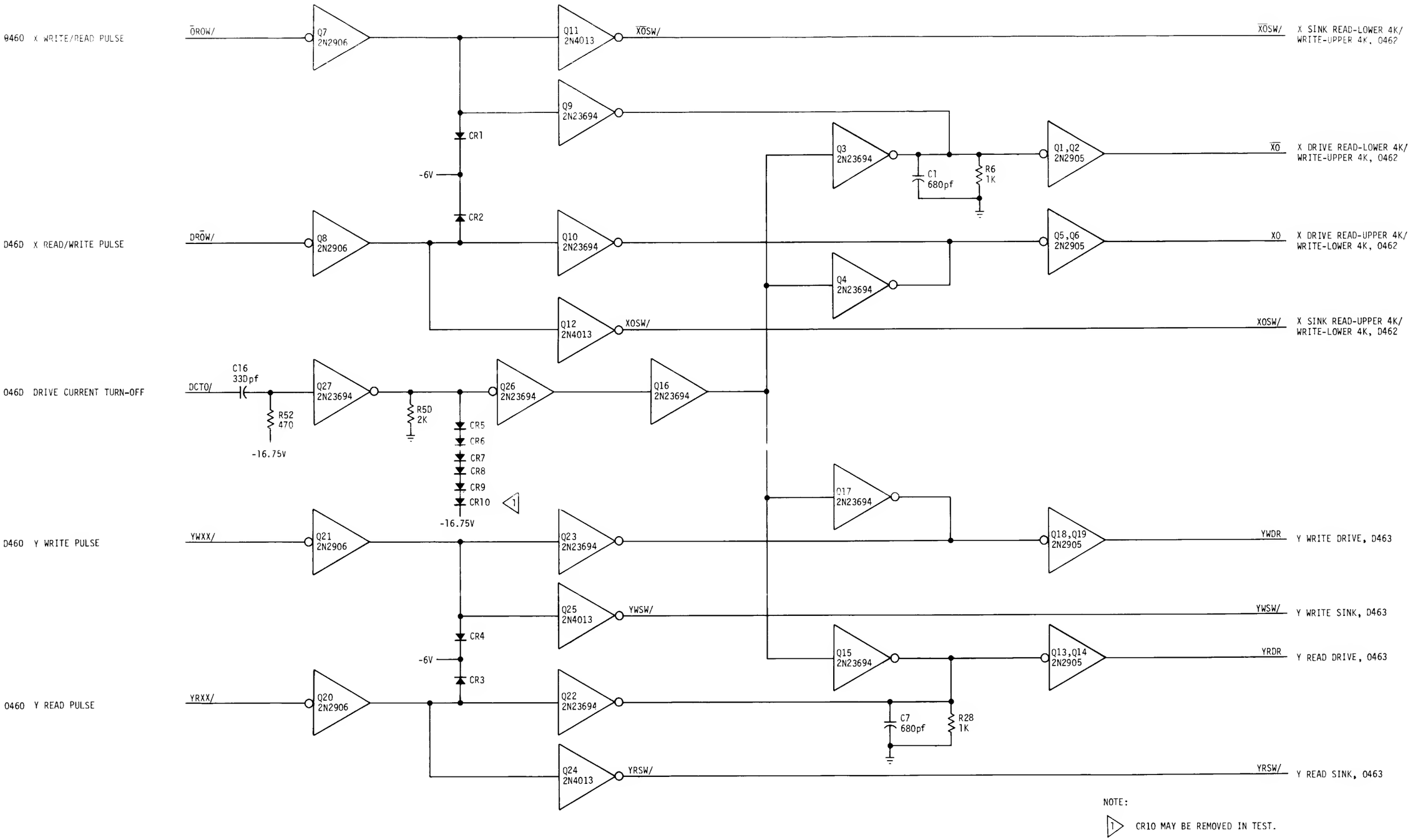
MO4A/ → Z3 9016

MEN, READ → Z7 9002

0451 READ ENABLE

READ → P1-B23

Z3 9016 → MSAR MEMORY SELECT AND READ, 0465, 0466, 0467, 0468



MEMORY DRIVE CIRCUITS

CORE MEMORY
0461

X SELECT BITS 0-7

0461 X DRIVE READ-UPPER 4K/ WRITE-LOWER 4K

0420 N REG BIT 0

PG iv N REG BIT 0

0420 N REG BIT 1

PG iv N REG BIT 1

0420 N REG BIT 2

PG iv N REG BIT 2

0460 ENABLE DECODER

0461 X SINK READ-LOWER 4K/ WRITE-UPPER 4K

0461 X SINK READ-UPPER 4K/ WRITE-LOWER 4K

0420 N REG BIT 5

PG iv N REG BIT 5

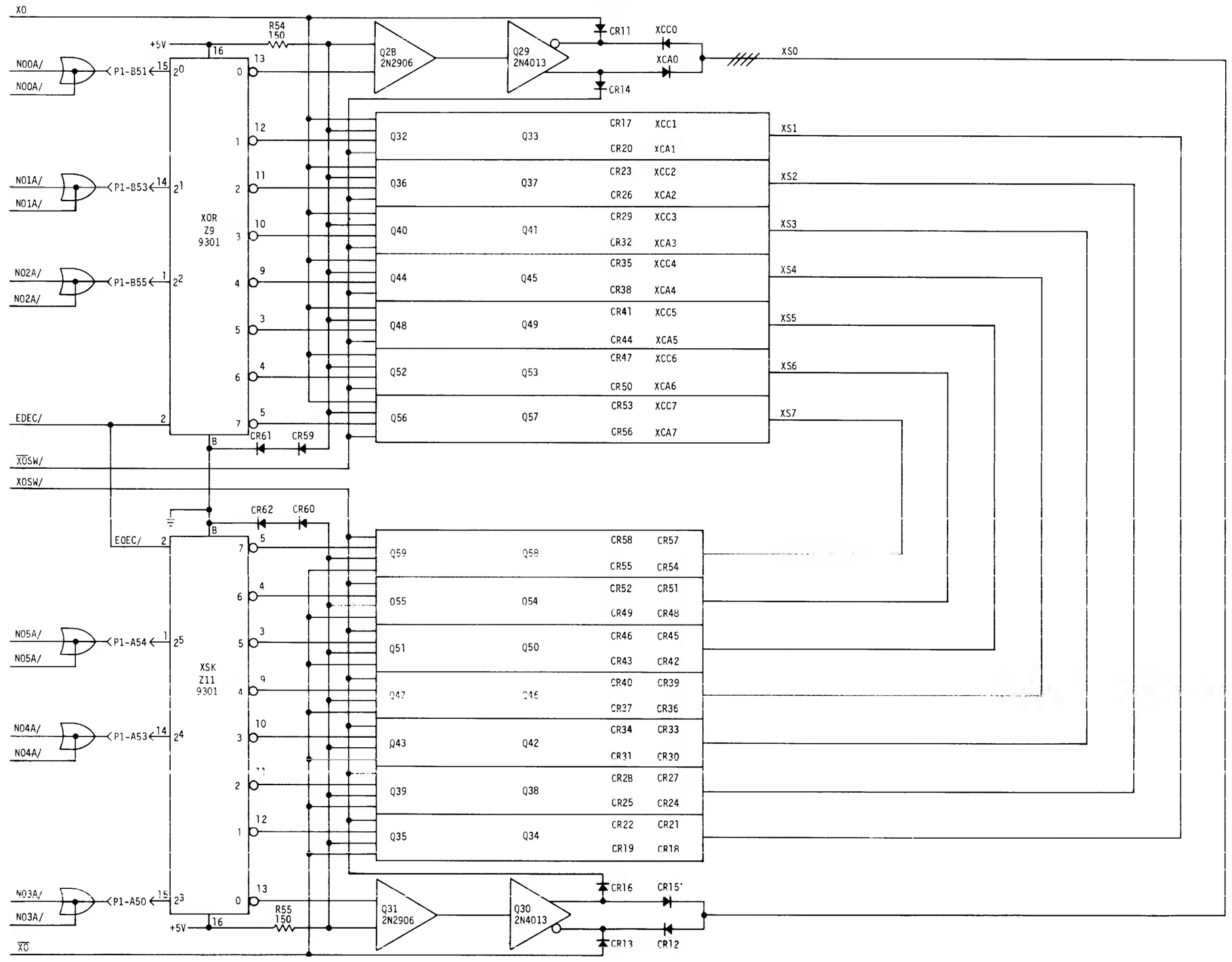
0420 N REG BIT 4

PG iv N REG BIT 4

0420 N REG BIT 3

PG iv N REG BIT 3

0461 X DRIVE READ-LOWER 4K/ WRITE-UPPER 4K



0461 Y WRITE DRIVE

0420 N REG BIT 6

PG iv N REG BIT 6

0420 N REG BIT 7

PG iv N REG BIT 7

0410 M REG BIT 0

PG iv M REG BIT 0

0460 ENABLE OECODER

0461 Y REAO SINK

0461 Y WRITE SINK

0410 M REG BIT 3

PG iv M REG BIT 3

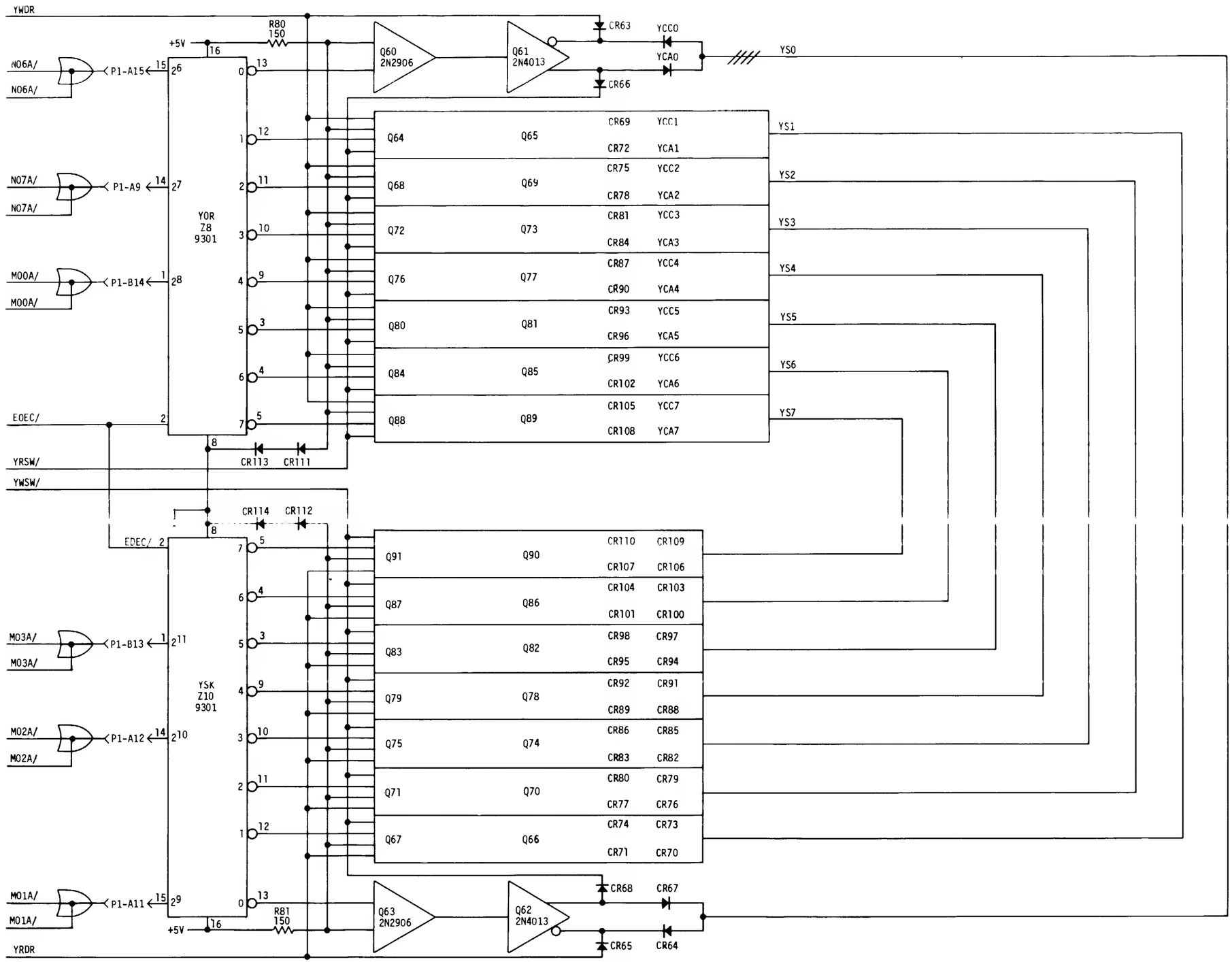
0410 M REG BIT 2

PG iv M REG BIT 2

0410 M REG BIT 1

PG iv M REG BIT 1

0461 Y REAO ORIVE



Y SELECT BITS 0-7

PRIORITY/SELECT, MEMORY CLAMP AND POWER

PRIORITY IN FROM A55 OF NEXT LOWER NUMBERED JACK (PROT/) — PRIN/ — P1-B54 — P1-A55 — PROT/ — PRIORITY OUT TO B54 OF NEXT HIGHER NUMBERED JACK (PRIN/)

SELECT IN FROM A52 OF NEXT LOWER NUMBERED JACK (SELO/) — SELI/ — P1-B52 — P1-A52 — SELO/ — SELECT OUT TO B52 OF NEXT HIGHER NUMBERED JACK (SELI/)

+5V

VTH — P1-B61

R136 511

GROUND — P1-A1, P1-A2, P1-A64, P1-A65

R137 2

C31 22 | C32 22 | C33 22 | C58 22 | C56 22 — +V REF

-V REF

CR164 5.1V

CR165

+ C20 47 | C34 0.01 | C35 0.01

Q110 2N2905

-5V

R133 1K | R134 1K | R135 68

-16.75V

C19 330 pf | C55 220 pf | R108 470 | R109 470

Q92,Q93 2N4013

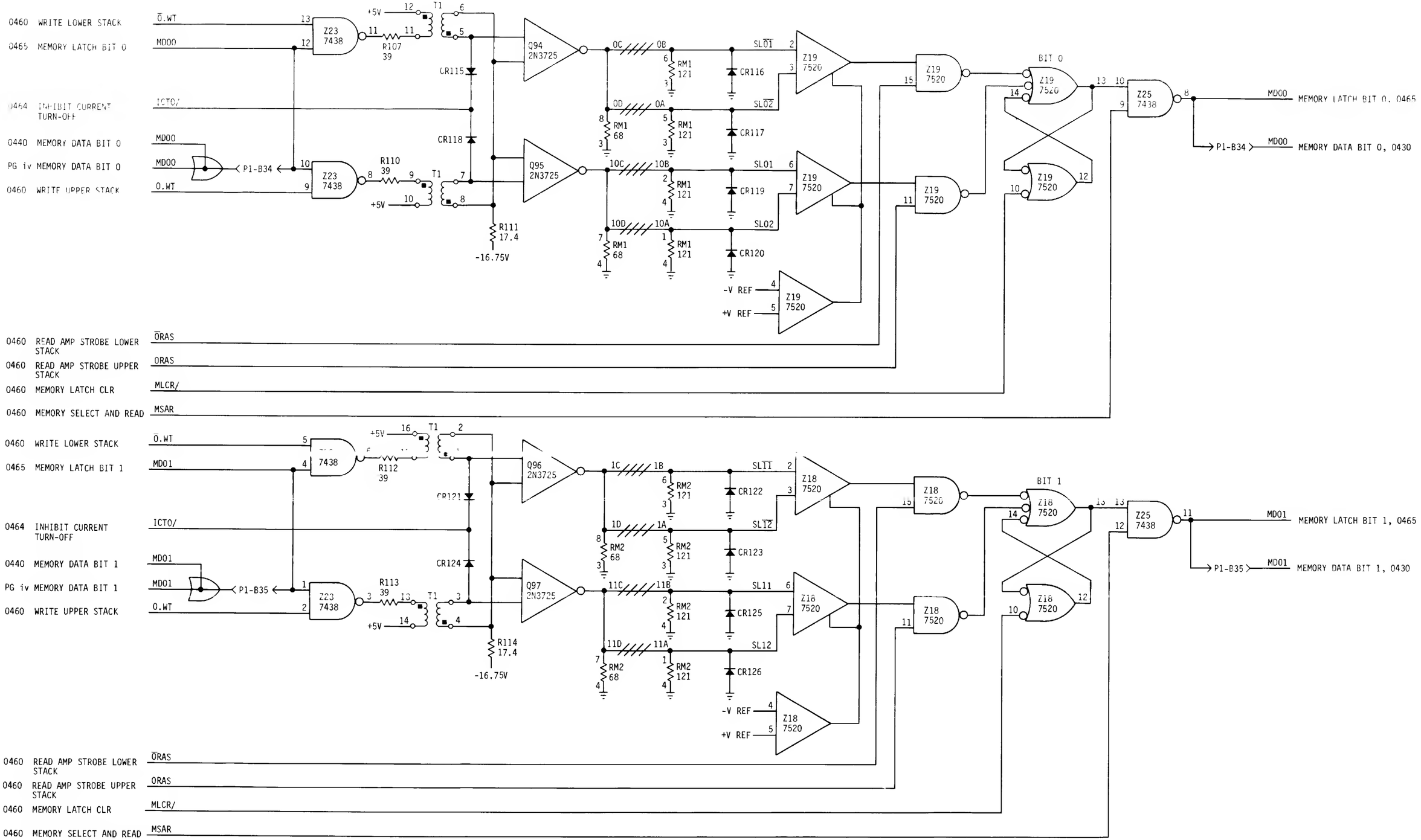
0460 INHIBIT CURRENT TURN-OFF — ICTO — ICTO/ — INHIBIT CURRENT TURN-OFF, 0465, 0466, 0467, 0468

+5 VOLTS — P1-B1, P1-B2, P1-B64, P1-B65

C13 22 | C14 22 | C17 0.01 | C18 0.10 | C21 0.01 | C22 0.01 | C36 4.7 | C37 4.7 | C38 0.01 | C39 0.01 | C46 0.01 | C47 0.01 | C52 4.7 | C53 4.7 | C48 0.01 | C49 0.01 | C50 0.01 | C51 0.01 — +5V

C40 22 | C41 22 | C42 22 | C43 22 | C44 22 | C45 22 | C57 22 | C2 22 | C12 22 | C54 0.01 | C6 0.01 | C11 0.01 — -V REF

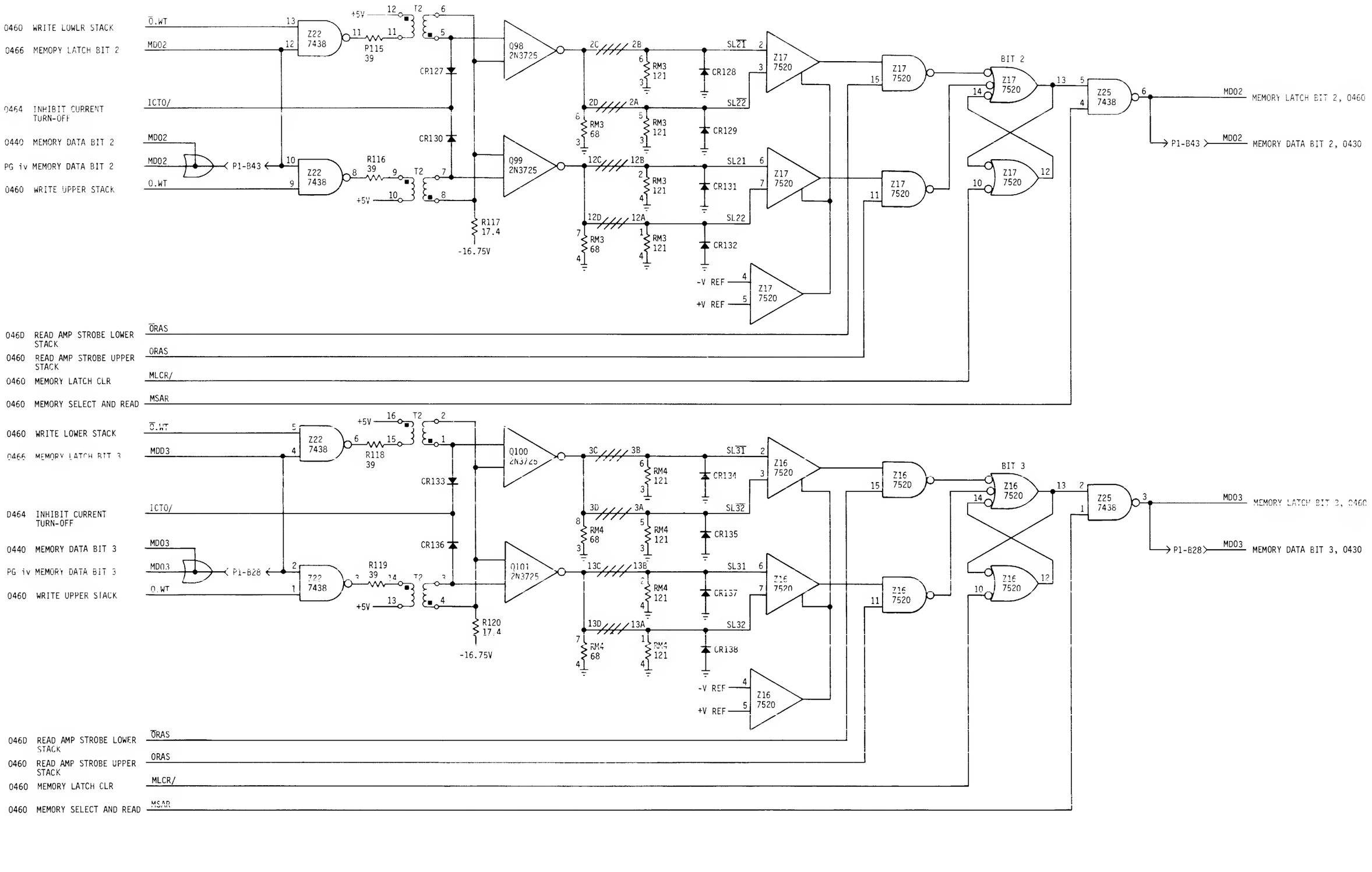
-16.75 VOLTS — P1-B3, P1-A4, P1-A63, P1-B63 — -16.75V

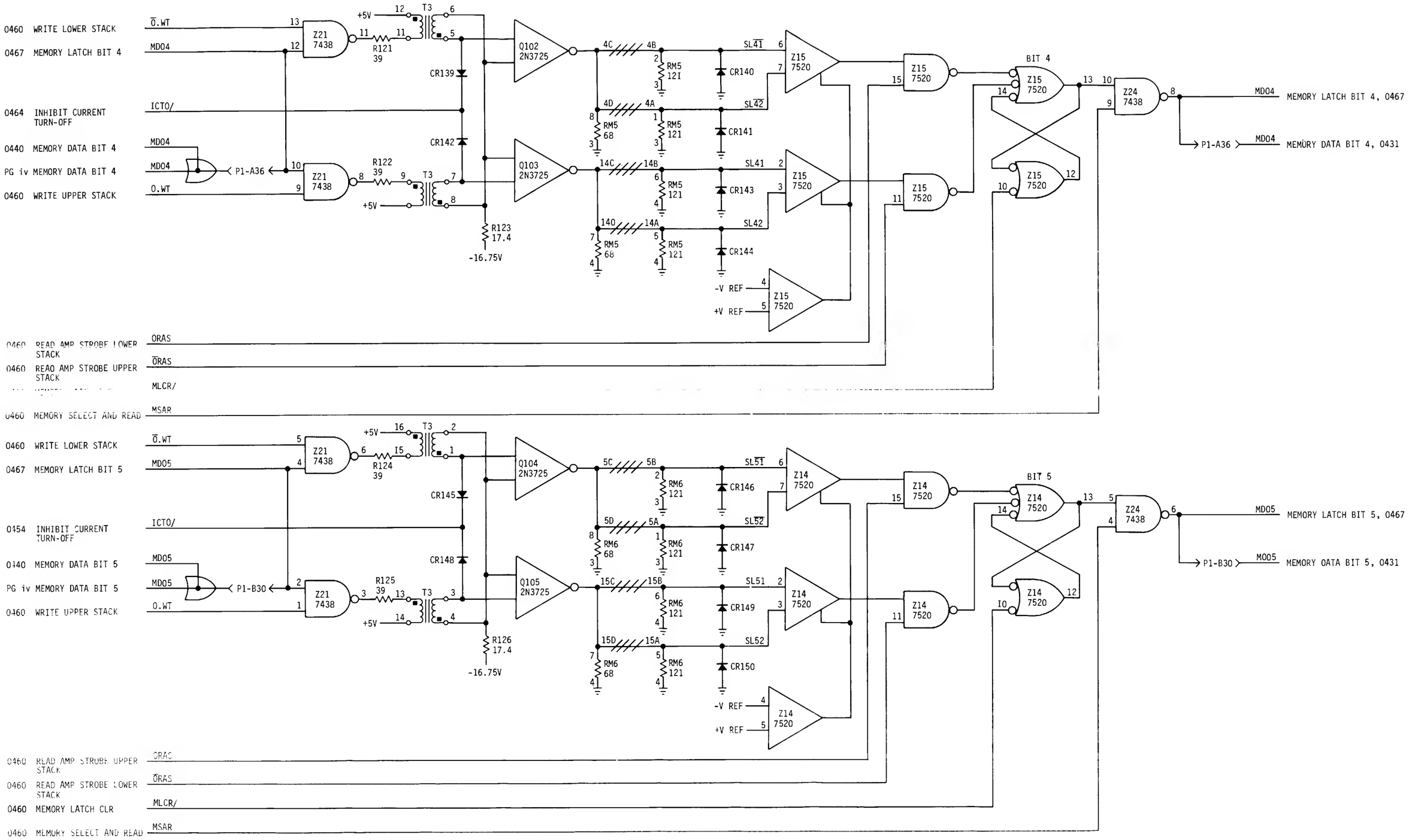


MEMORY READ/WRITE BITS 0 AND 1

CORE MEMORY
0465

MEMORY READ/WRITE BITS 2 AND 3

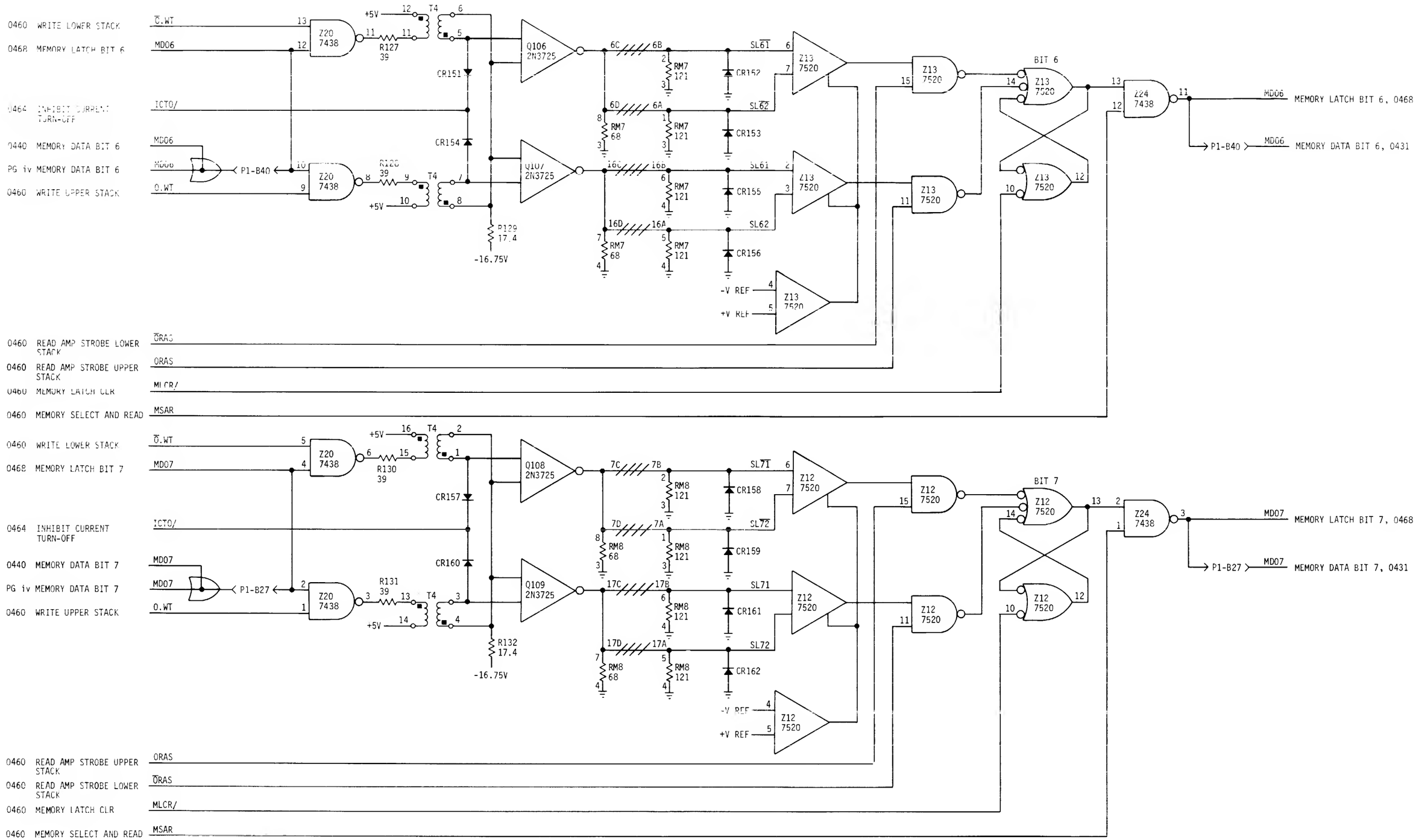


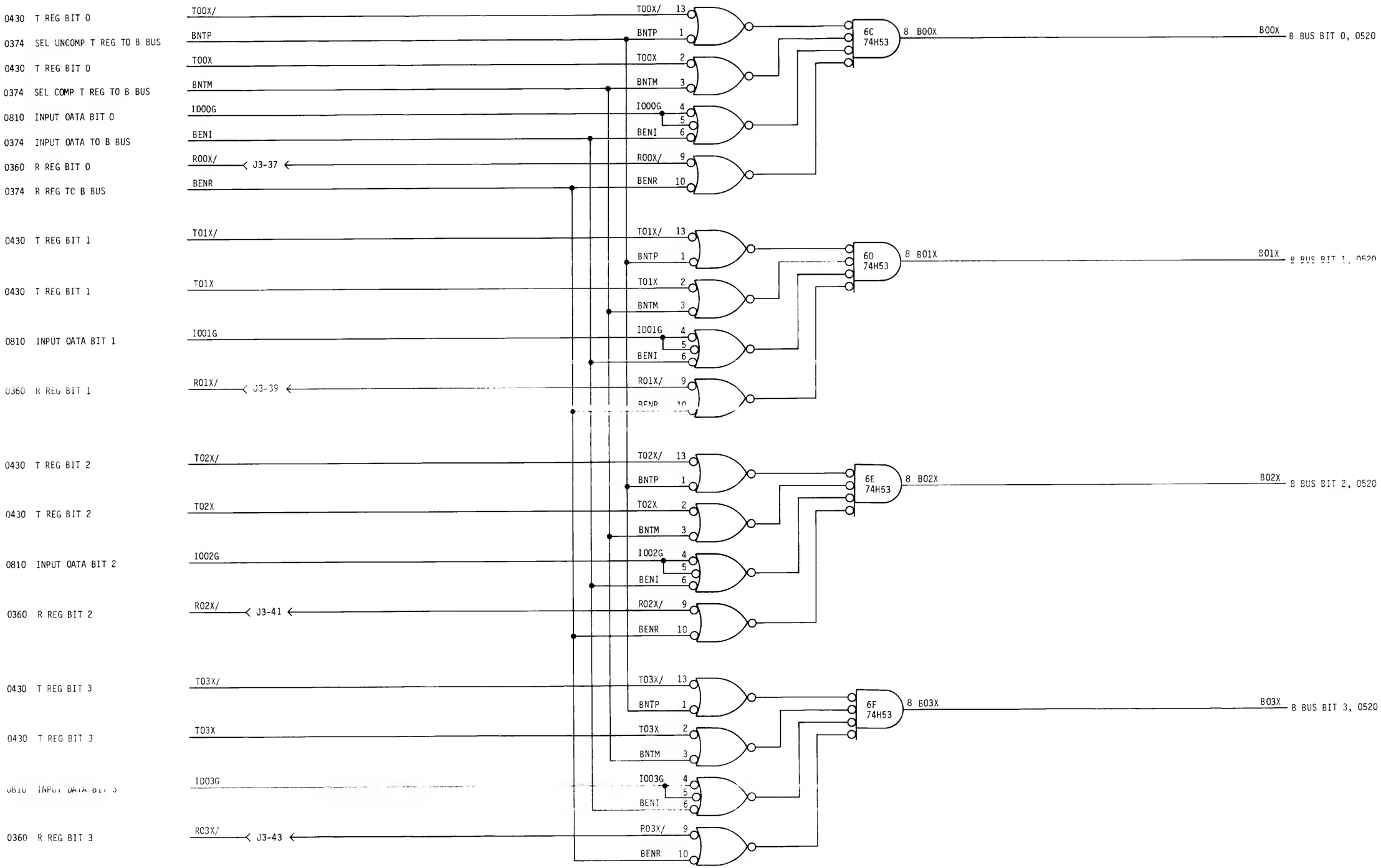


MEMORY READ/WRITE BITS 4 AND 5

CORE MEMORY
0467

MEMORY READ/WRITE BITS 6 AND 7

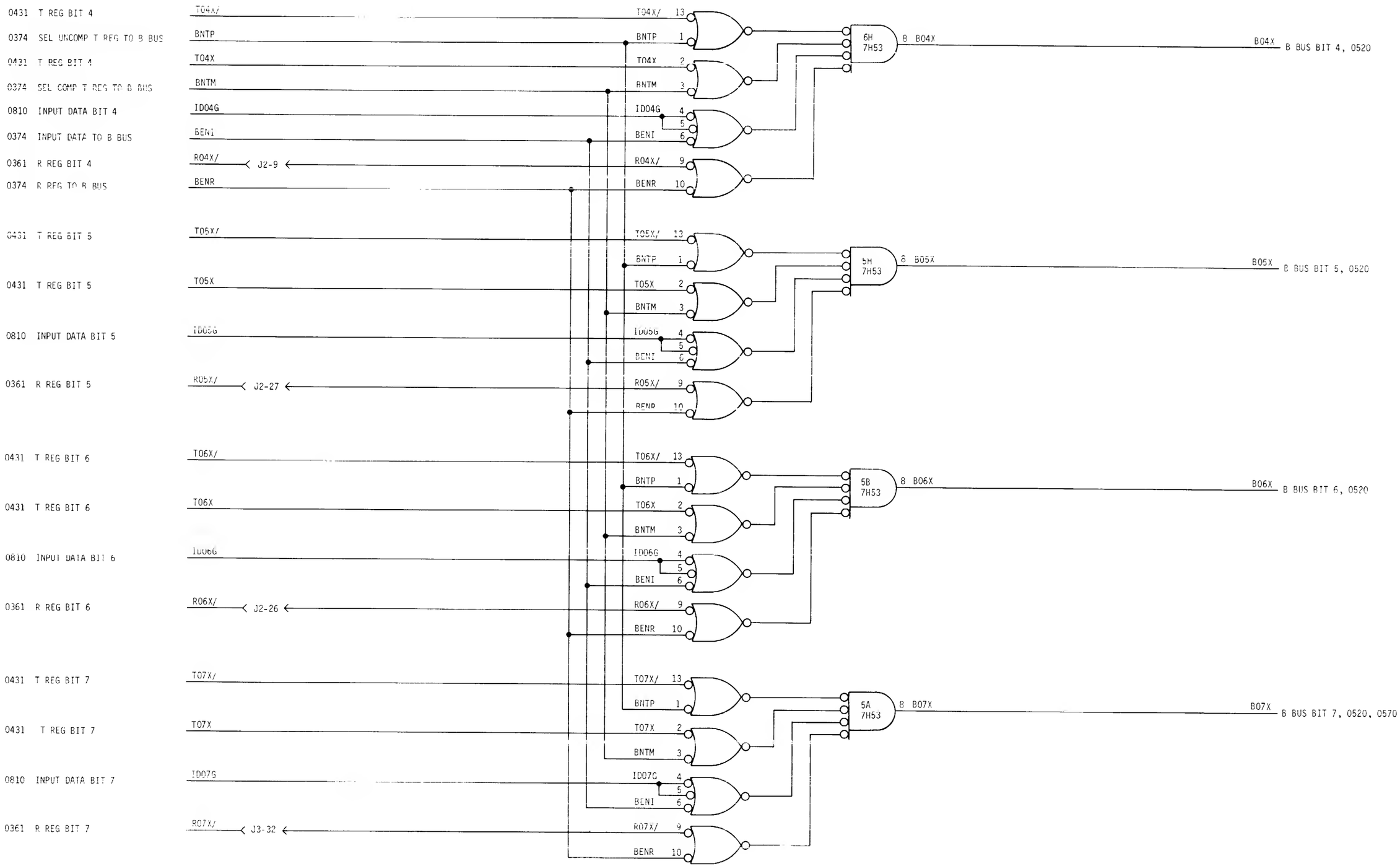




B BUS MULTIPLEXER BITS 0-3

J3 DATA BOARD
0510

B BUS MULTIPLEXER BITS 4-7



0560 INITIAL CARRY

0550 FILE BIT 0

0510 B BUS BIT 0

0550 FILE BIT 1

0510 B BUS BIT 1

0550 FILE BIT 2

0510 B BUS BIT 2

0550 FILE BIT 3

051D B BUS BIT 3

0550 FILE BIT 4

0511 B BUS BIT 4

0550 FILE BIT 5

0511 B BUS BIT 5

0550 FILE BIT 6

0511 B BUS BIT 6

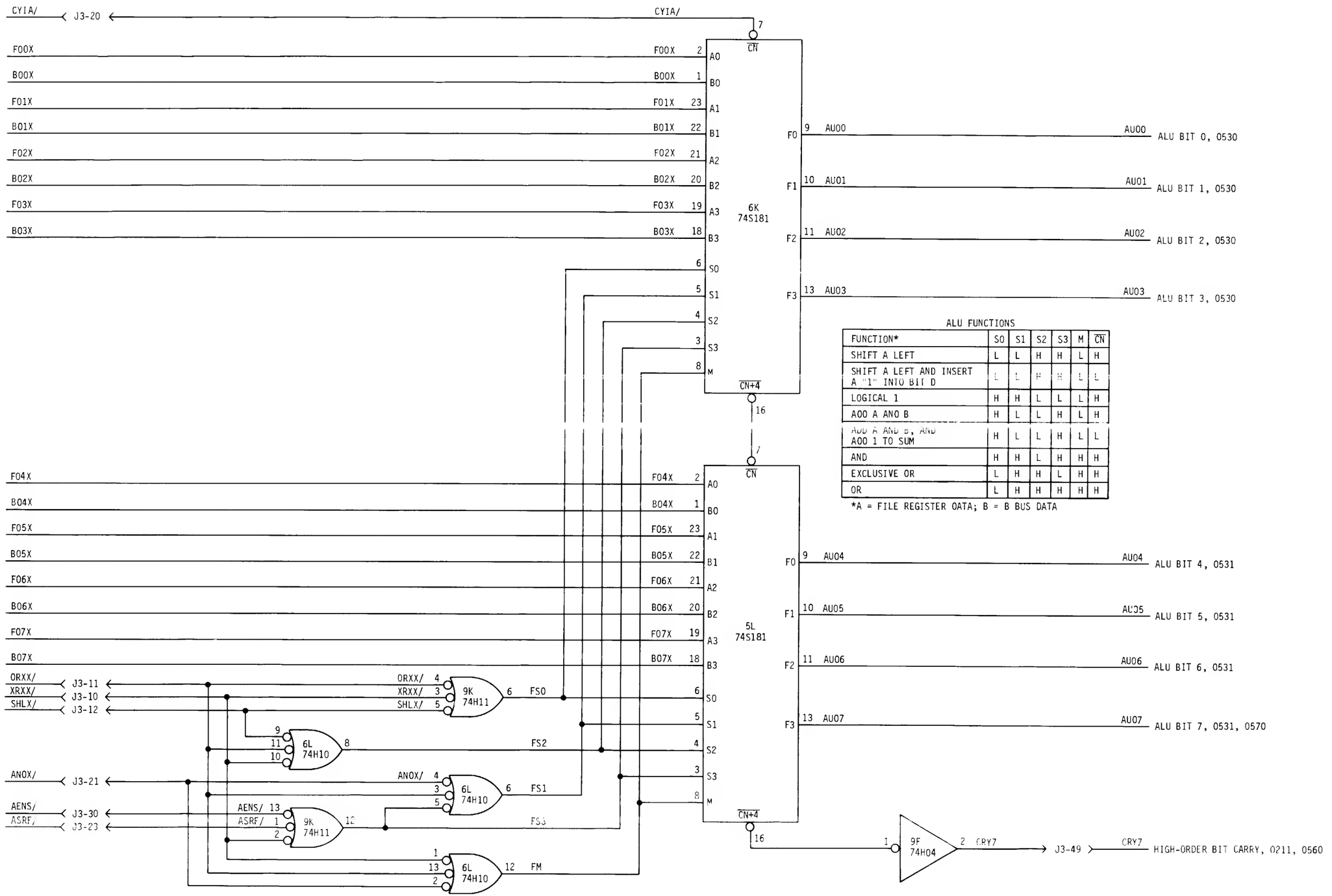
0550 FILE BIT 7

0511 B BUS BIT 7

0370 OR COMMAND
0370 EXCLUSIVE OR COMMAND
0372 SHIFT LEFT

0372 LOGICAL AND

0373 ENTER SENSE SWITCHES
0373 SHIFT FILE RIGHT 4



ALU FUNCTIONS

FUNCTION*	S0	S1	S2	S3	M	$\overline{CN}$
SHIFT A LEFT	L	L	H	H	L	H
SHIFT A LEFT AND INSERT A "1" INTO BIT D	L	L	H	H	L	L
LOGICAL 1	H	H	L	L	L	H
A00 A AND B	H	L	L	H	L	H
ADD A AND B, AND A00 1 TO SUM	H	L	L	H	L	L
AND	H	H	L	H	H	H
EXCLUSIVE OR	L	H	H	L	H	H
OR	L	H	H	H	H	H

*A = FILE REGISTER OATA; B = B BUS DATA

ARITHMETIC/LOGIC UNIT

J3 DATA BOARD
0520

A BUS MULTIPLEXER BITS 0-3

0210 PANEL INTERRUPT CONTROL
0550 FILE BIT 1
0550 FILE BIT 4
0520 ALU BIT 0
PG iv DMA TERMINATION
0550 FILE BIT 2
0550 FILE BIT 5
0520 ALU BIT 1
0373 SHIFT FILE RIGHT 4
0373 ENTER INTERNAL STATUS
0373 SHIFT RIGHT
0630 RFAL TIME CLOCK INTERRUPT
0550 FILE BIT 3
0550 FILE BIT 6
0520 ALU BIT 2
SPARE STATUS LINE
0550 FILE BIT 4
0550 FILE BIT 7
0520 ALU BIT 3

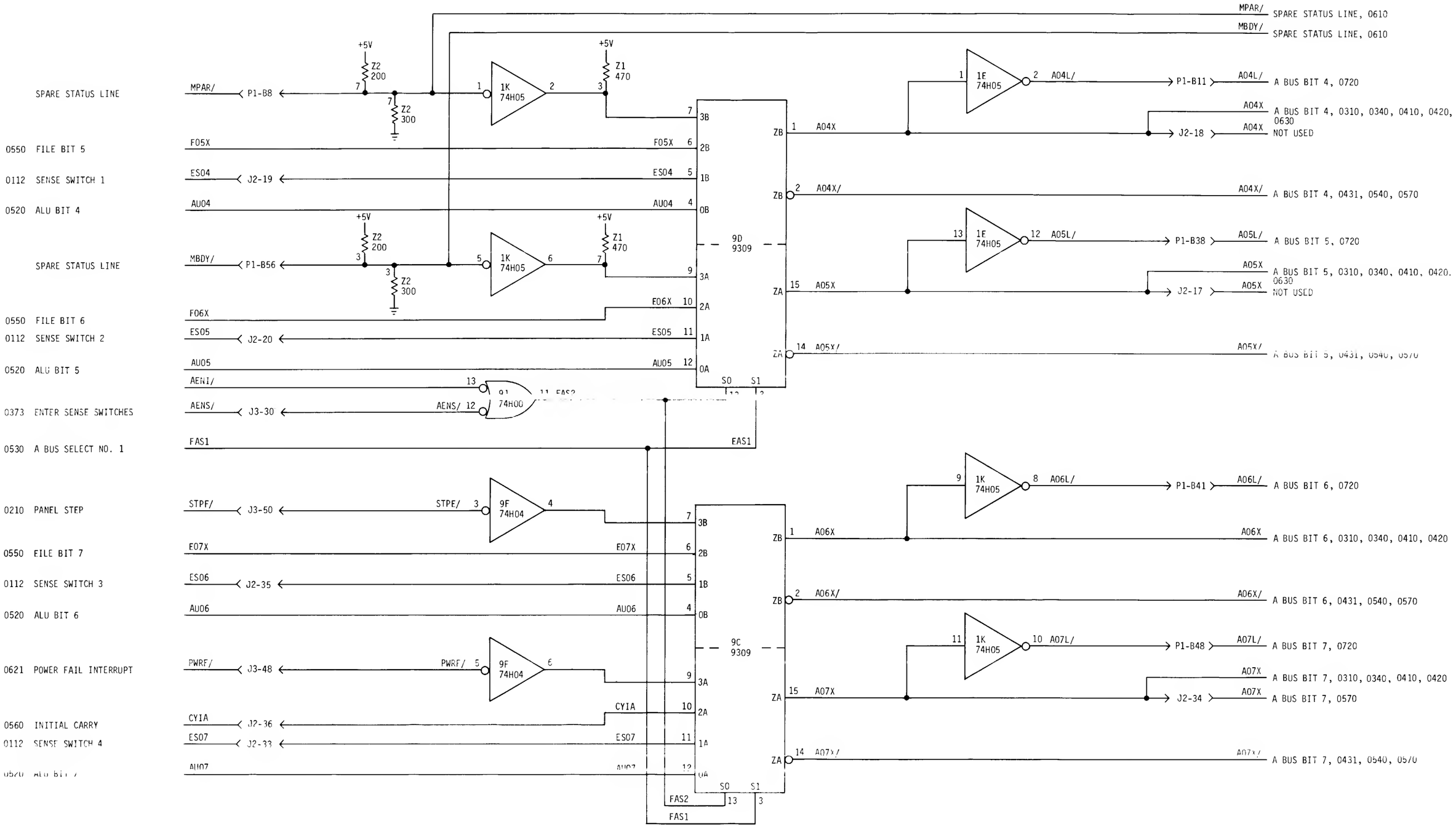
INTC/ < J2-39
F01X
F04X
AU00
SPARE/ < P1-B49
F02X
F05X
AU01
ASRF/ < J3-23
AEN1/ < J3-27
SHRX/ < J3-26
RTCI/ < J3-44
F03X
F06X
AU02
MPRO < P1-B57
F04X
F07X
AU03

8H 74H05
8L 74H05
9J 74H00
9J 74H00
8H 74H05
1K 74H05
R2 470
R7 470
R6 470
R1 470
Z2 200
Z2 300
Z2 200
Z2 300
+5V

8H 9309
9E 9309
S0 S1
FAS0
FAS1

1F 74H05 → P1-A13 → A00L/ A BUS BIT 0, 0710
A00X A BUS BIT 0, 0310, 0340, 0410, 0420
A00X/ A BUS BIT 0, 0570, 0540, 0430
1F 74H05 → P1-A14 → A01L/ A BUS BIT 1, 0710
A01X A BUS BIT 1, 0310, 0340, 0410, 0420
A01X/ A BUS BIT 1, 0430, 0540, 0570
1F 74H05 → P1-A29 → A02L/ A BUS BIT 2, 0710
A02X A BUS BIT 2, 0310, 0340, 0410, 0420
J2-2 → A02X A BUS BIT 2, 0610
A02X/ A BUS BIT 2, 0430, 0540, 0570
1F 74H05 → P1-A34 → A03L/ A BUS BIT 3, 0710
A03X A BUS BIT 3, 0310, 0340, 0410, 0420
J2-1 → A03X A BUS BIT 3, 0610
A03X/ A BUS BIT 3, 0430, 0540, 0570

SPARE/ DMA TERMINATION, 0610
FAS1 A BUS SELECT NO. 1, 0531
MPRO/ SPARE STATUS LINE, 0610



A BUS MULTIPLEXER BITS 4-7

J3 DATA BOARD
0531

FILE REGISTERS AND FILE ZERO FLAGS

0550 SELECT SECONDARY FILE
0362 R REG BIT 8-11
0530 A BUS BIT 0-3
0531 A BUS BIT 4-7

0550 SELECT PRIMARY FILE
0230 FILE WRITE CLOCK

0570 OVERFLOW CONDITION

0570 NEGATIVE CONDITION

0570 ZERO CONDITION

PG iv CONCURRENT I/O REQUEST

0610 INTERNAL STATUS INTERRUPT

SPARE STATUS LINE

NOT USED

0610 EXT INTERRUPT REQUEST

055C SELECT FILE ZERO

J3 DATA BOARD

FBS2/
R08X-R11X
A00X/-A03X/
A04X/-A07X/
FBS1/
CLK2/ — J3-22
CC0X/ — J2-3
CC1X/ — J3-31
CC2X/ — J2-4
ECIO/ — P1 B42
INTL/
IRPY/ — P1-B50
TTIN/ OR STOV/ — P1-B46 — J3-46 — J3-46
INTR/ — J3-47
FAZO

+5V
Z11 200
Z11 300

J2 CONTROL BOARD

FILE ZERO FLAGS

8E 7438: CC0X/ 1, 2 → 3 F00Z
8E 7438: CC1X/ 12, 13 → 11 F01Z
8E 7438: CC2X/ 9, 10 → 8 F02Z
8E 7438: ECIO/ 4, 5 → 6 F03Z
8F 7438: INTL/ 1, 2 → 3 F04Z
8F 7438: IRPY/ 12, 13 → 11 F05Z
8F 7438: TTIN/ OR STOV/ 9, 10 → 8 F06Z
8F 7438: INTR/ 4, FAZO 5 → 3 F07Z

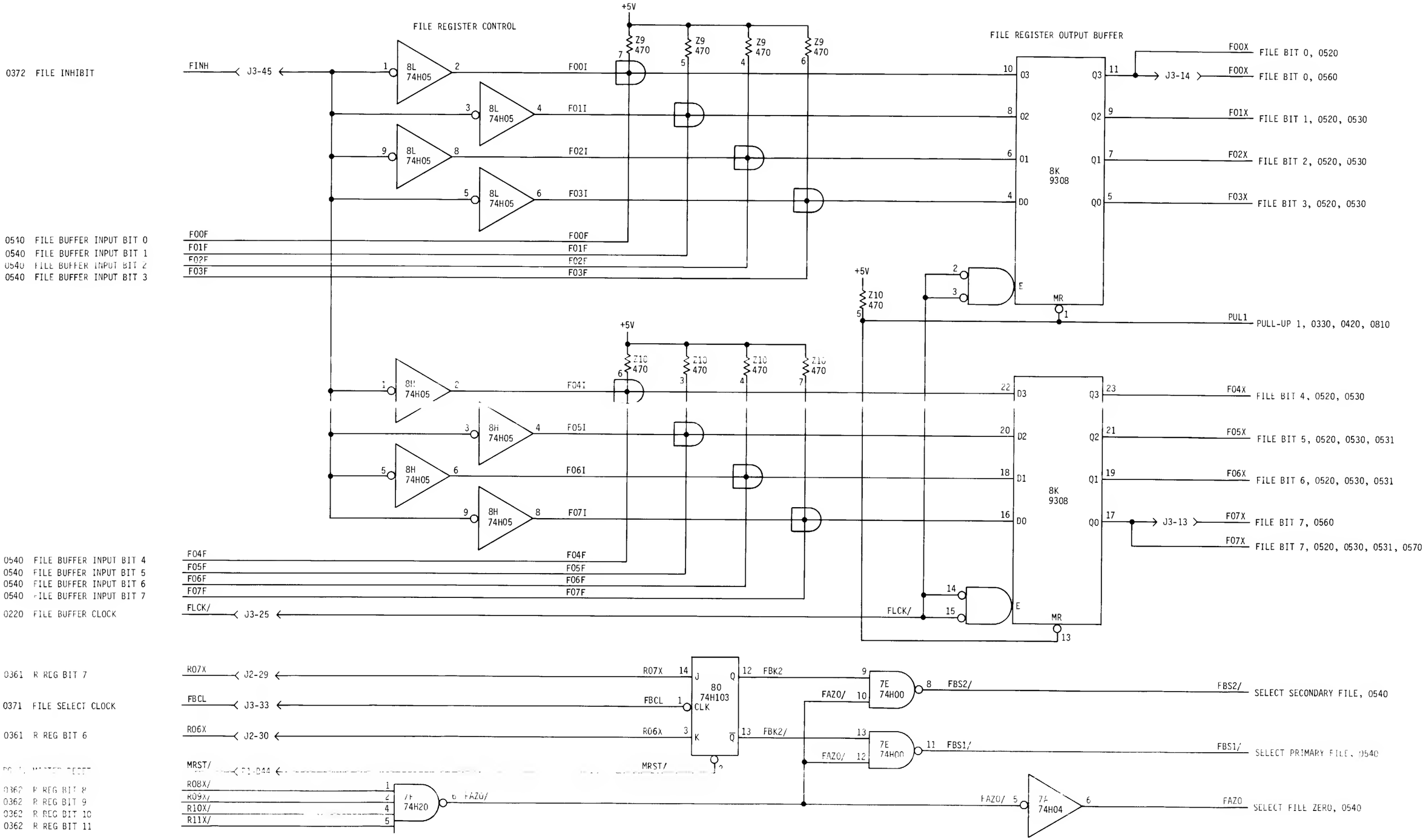
PRIMARY FILE

7K P3101A: R08X 1, R09X 15, R10X 14, R11X 13, A00X/ 4, A01X/ 6, A02X/ 10, A03X/ 12, FBS1/ 2, CLK2/ 3 → Q1 5 F00P, Q2 7 F01P, Q3 9 F02P, Q4 11 F03P
7J P3101A: R08X 1, R09X 15, R10X 14, R11X 13, A04X/ 4, A05X/ 6, A06X/ 10, A07X/ 12, F8S1/ 2, CLK2/ 3 → Q1 5 F04P, Q2 7 F05P, Q3 9 F06P, Q4 11 F07P

SECONDARY FILE

7L P3101A: R08X 1, R09X 15, R10X 14, R11X 13, A00X/ 4, A01X/ 6, A02X/ 10, A03X/ 12, FBS2/ 2, CLK2/ 3 → Q1 5 F00S, Q2 7 F01S, Q3 9 F02S, Q4 11 F03S
7H P3101A: R08X 1, R09X 15, R10X 14, R11X 13, A04X/ 4, A05X/ 6, A06X/ 10, A07X/ 12, F8S2/ 2, CLK2/ 3 → Q1 5 F04S, Q2 7 F05S, Q3 9 F06S, Q4 11 F07S

F00F FILE BUFFER INPUT BIT 0, 0550
F01F FILE BUFFER INPUT BIT 1, 0550
F02F FILE BUFFER INPUT BIT 2, 0550
F03F FILE BUFFER INPUT BIT 3, 0550
F04F FILE BUFFER INPUT BIT 4, 0550
F05F FILE BUFFER INPUT BIT 5, 0550
F06F FILE BUFFER INPUT BIT 6, 0550
F07F FILE BUFFER INPUT BIT 7, 0550



FILE REGISTER CONTROL AND FILE REGISTER OUTPUT BUFFER

LINK REGISTER AND INITIAL CARRY LOGIC

0550 FILE BIT 7
0372 SHIFT LEFT
0550 FILE BIT 0
0373 SHIFT RIGHT
0370 SHIFT FILE
0520 HIGH-ORDER BIT CARRY
0370 SHIFT FILE

0370 ADD COMMAND
0370 COMPARE FILE
0370 SUBTRACT COMMAND
0372 M OR N REG SELECT

0230 DATA CLOCK

0570 CLAMP
0372 M OR N REG SELECT

0370 SUBTRACT COMMAND
0361 R REG BIT 6
0361 R REG BIT 7

0370 MEMORY READ OR WRITE
0361 R REG BIT 6

0370 MEMORY READ OR WRITE
0361 R REG BIT 7

0363 R REG BIT 15
0560 SEL LINK BIT

0374 CODE 01 IN C FIELD BITS 7 AND 6

0360 R REG BIT 0
0360 R REG BIT 1
0360 R REG BIT 2

LINK REGISTER

FO7X ← J3-13 (1)
SHLX (13)
FOOX ← J3-14 (10)
SHRX (9)
SHXX
CRY7 ← J3-49
SHXX/

5L 74H51
6L 74H04
SHCY → J2-50 → SHCY — OUT-SHIFTED FILE BIT, 0570

SHXX (4)
CRY7 (2)
SHXX/ (3)
5L 74H51

ARITH LINK
PRESET, 4K 74H74
ARTL/ → P1-B62 → ARTL/ — NOT USED

+5V
R42 220

4F 7438
7H 74H04
LINK → SEL LINK BIT, 0560

ADXX/
CPXX/
SBXX/
6J 74H20
SACS
4J 74H10

P1-B61 → LINK/ — NOT USED
P1-B60 → MALK/ — NOT USED
P1-A60 → MNPX/ — NOT USED
P1-A61 → EALC — NOT USED
P1-A62 → SACS — NOT USED

MNRX/

MEMORY LINK
PRESET, 4K 74H74

CLK1
SACS
MNRX
4J 74H10
ARTC/

CLAMP
MNRX

+5V
R54 470

INITIAL CARRY LOGIC

SBXX
RO6X/
RO7X/
7K 74H22

MYXX/
RO6X
7L 74H22

MYXX
RO7X
7L 74H22

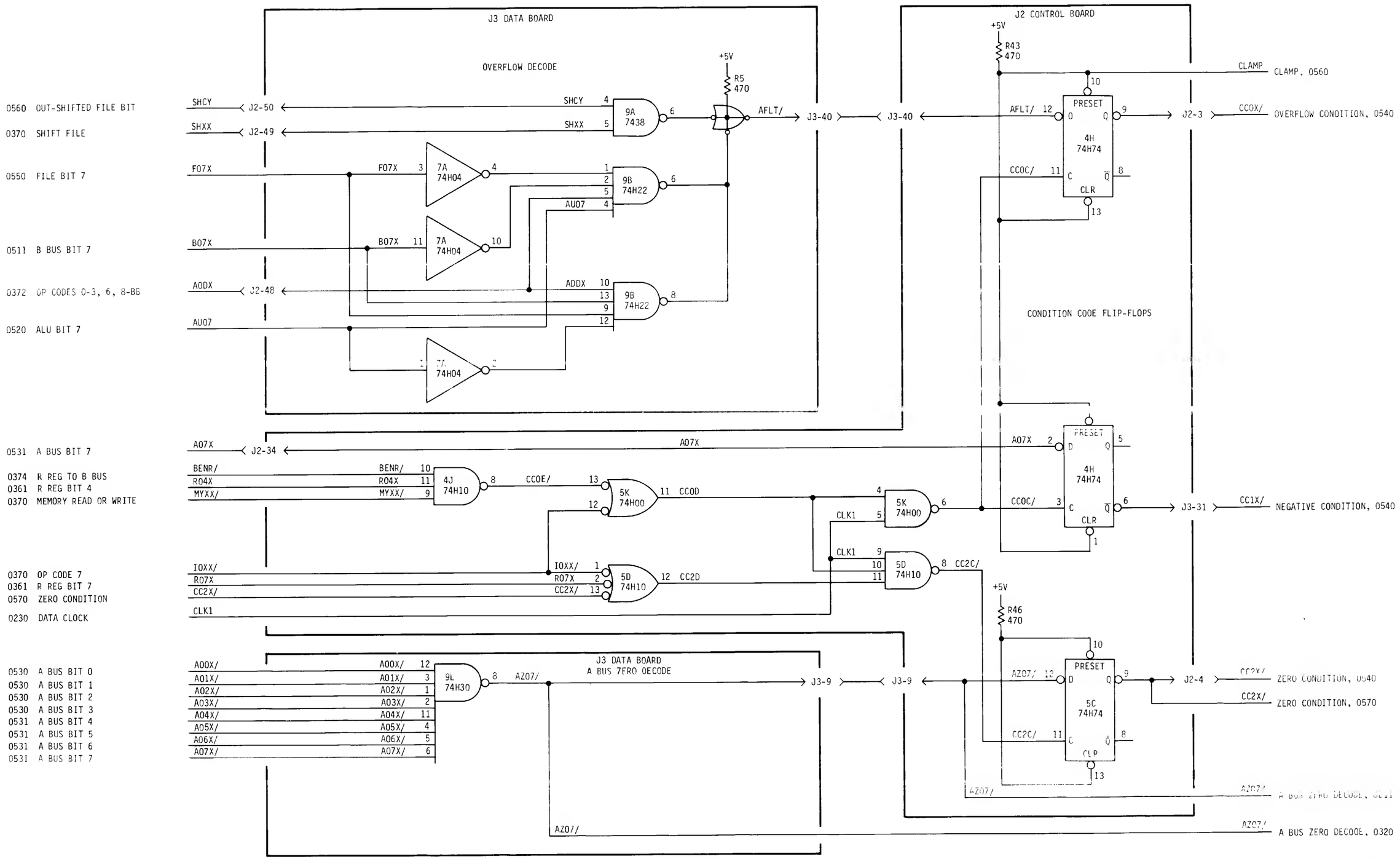
R15X
LINK
7K 74H22

MYDX
7J 74H22

R00X/
R01X
R02X/
6H 74H11

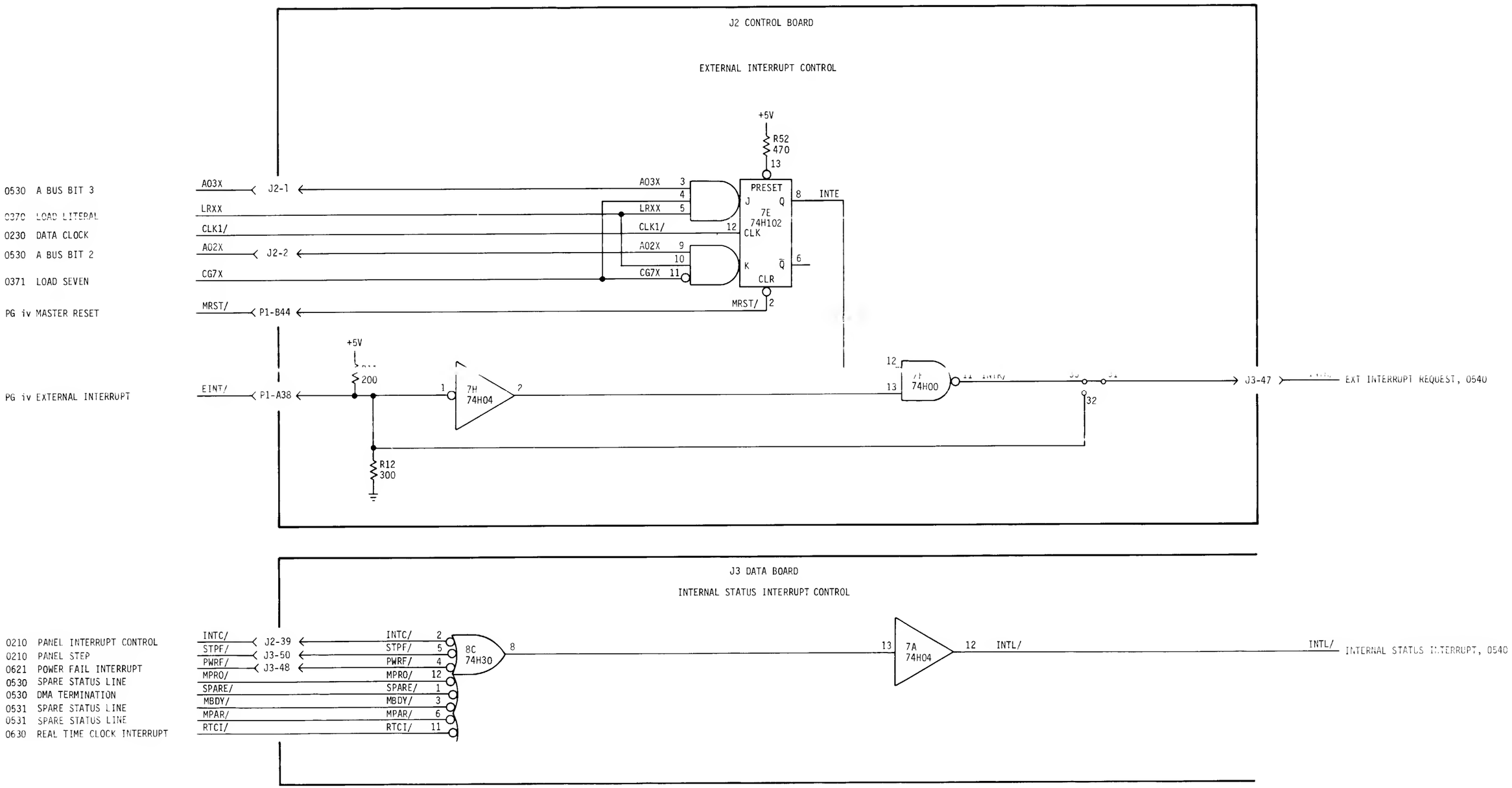
CYIA/ 13 → 8L 74H04 → 12 → J2-36 → CYIA — INITIAL CARRY, 0531
J3-20 → CYIA/ — INITIAL CARRY, 0520

NOTE:
1. JUMPER CONNECTIONS FOR SEPARATE MEMORY AND ARITHMETIC LINK IS SHOWN. FOR COMBINED MEMORY AND ARITHMETIC LINK, PAD 1 IS JUMPERED TO PAD 2, AND PAD 5 IS JUMPERED TO PAD 6, AND JUMPERS BETWEEN PADS 2 and 3, AND BETWEEN PADS 4 AND 6 ARE REMOVED. WHEN EXTERNAL MEMORY/ARITHMETIC LINK SWITCH IS INCLUDED JUMPERS BETWEEN PADS 2 AND 3 AND BETWEEN PADS 4 AND 6 ARE REMOVED.



OVERFLOW DECODE, A BUS ZERO DECODE AND CONDITION CODE FLIP-FLOPS

J2 CONTROL BOARD
AND J3 DATA BOARD
0570



INTERNAL AND EXTERNAL INTERRUPTS

J2 CONTROL BOARD
AND J3 DATA BOARD
0610

POWER FAIL 1

0620 POWER FAIL STATE 0
0621 RESET POWER FAIL SEQUENCER
0220 5-MHZ CLOCK PHASE 1
0620 POWER FAIL STATE 2
0620 POWER FAIL STATE 1
0620 POWER FAIL STATE 3
2010 POWER FAILURE DETECT
0211 RUN STATE
0211 RUN STATE
0620 POWER FAIL STATE 4
0620 POWER FAIL STATE 0

PFS0
PFRS/
SCK6
PFS2
PFS1
PFS3
PWRD/ P1-A3
RUNX/
RUNX
PFS4
PFS0

3A 74164
1C 74H04
2A 74H05
4D 74H00
2B 7438
1A 9602
1B 9602
1D 7438
4A 74H05

R21 470
R15 47K
C6 0.025
R1 100
C9 1.5
C8 0.1
R38 470
R37 470
R1/ 470

PFS1 POWER FAIL STATE 1, 0620
PFS2 POWER FAIL STATE 2, 0620
PFS3 POWER FAIL STATE 3, 0620
PFS4 POWER FAIL STATE 4, 0620
PFS0 POWER FAIL STATE 0, 0620
SPWF/ SET POWER FAIL INTERRUPT, 0621
RSTE/ ENABLE RESET ONE-SHOT, 0621
SPFS START POWER FAIL SEQUENCE, 0621

0620 START POWER FAIL SEQUENCE

SPFS

1B 7413

CR2 FDH600

+5V R25 330

CR3 FDH600

+5V R26 220

Q1 2N2369

PFRS/ RESET POWER FAIL SEQUENCER, 0620

CR4 FDH600

+5V R27 100

Q2 2N3725

P1-B44 MRST/ MASTER RESET, 0112

+5V R16 27K

C7 22

1A 9602

RSTE/

CLR

CR1

+5V R23 6.8K

C14 68

R24 5.1K

0620 SET POWER FAIL INTERRUPT

SPWF/

PRESET D Q CLR

3K 74H74

PWRF

3F 74H05

RUNF/

P1-A7 RUNF/ PANEL RUN, 0111

0230 DATA CLOCK

CLK1/

0373 ENTER INTERNAL STATUS

AENI

6F 74H00

PWRF/

J3-48 PWRF/ POWER FAIL INTERRUPT, 0531, 0610

PG iv MASTER RESET

MRST/

P1-B44

REAL TIME CLOCK

PG iv MASTER RESET

0373 ENTER INTERNAL STATUS

0211 CLOCK STOP

0630 LOAD RTC

0630 RESET INTERRUPT

0230 5-MHZ CLOCK PHASE 2

PG iv MASTER RESET

0531 A BUS BIT 5

0371 LOAD SEVEN

0370 LOAD LITERAL

0230 DATA CLOCK

0531 A BUS BIT 4

PG iv MASTER RESET

MRST/ ← P1-B44

AENI

CSTP/

RTCW/

RTCK/

2J 74H11

6A 9022

PRESET

CLK

K

CLR

RTC1/ → J3-44 → RTCI/ REAL TIME CLOCK INTERRUPT, 0530, 0610

R50 470

+5V

Z2 1K

CLK6/

6A 9022

RTCC

6C 74161

LD

A

B

C

D

CLR

QA

QB

QC

QD

CLK

CET

CEP

CARRY

RTC1

Z1 1K

6D 74161

RTC2

Z3 1K

6E 74161

NOTE:
JUMPER CONNECTIONS SHOWN ARE FOR A REAL TIME CLOCK INTERRUPT RATE OF 1 KHz

A05X ← J2-17

CG7X

LRXX

CLK1/

7D 74H102

A04X ← J2-18

MRST/ ← P1-B44

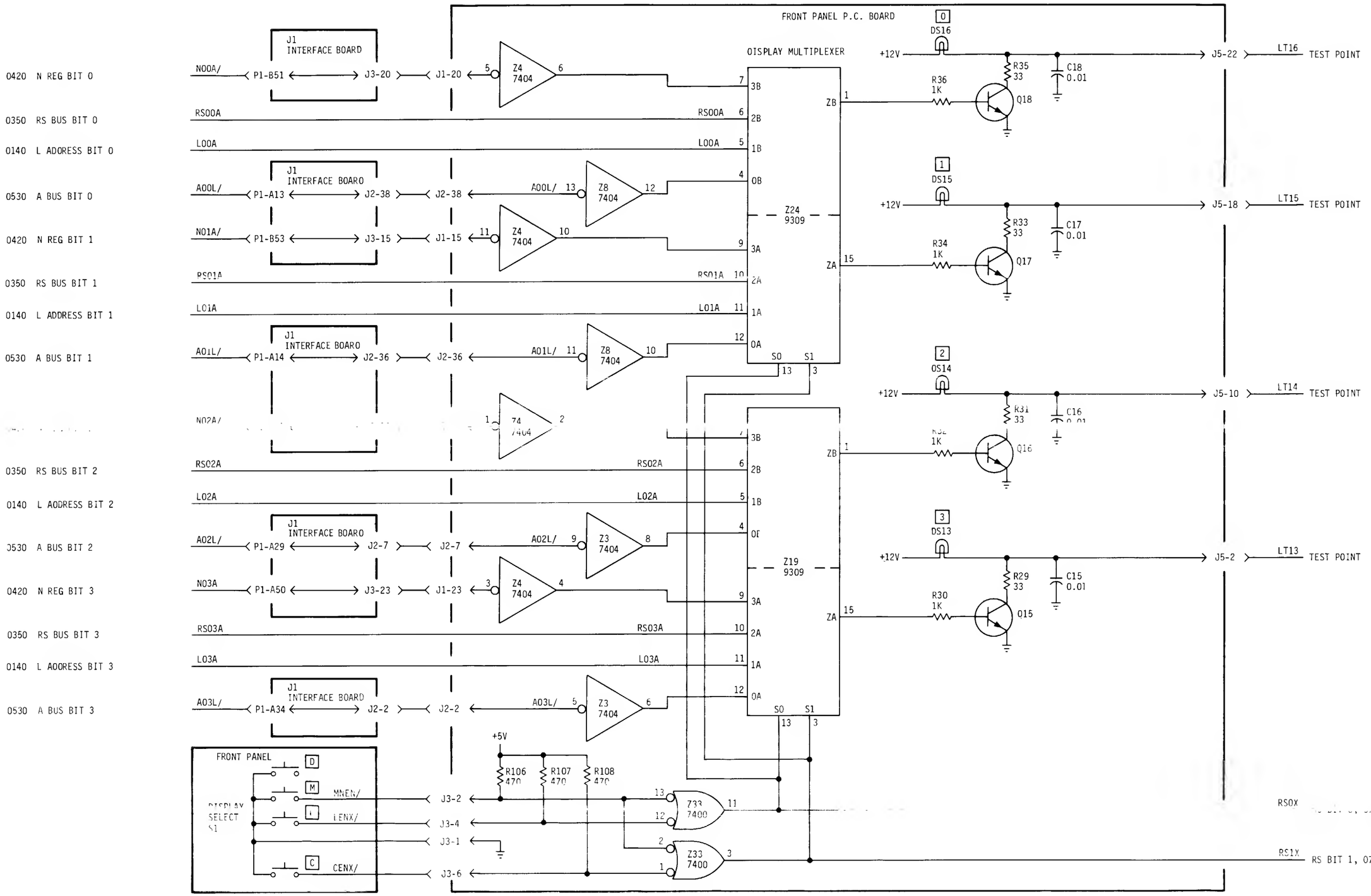
RTC3

5H 74H04

6F 74H00

RTCW/ LOAD RTC, 0630

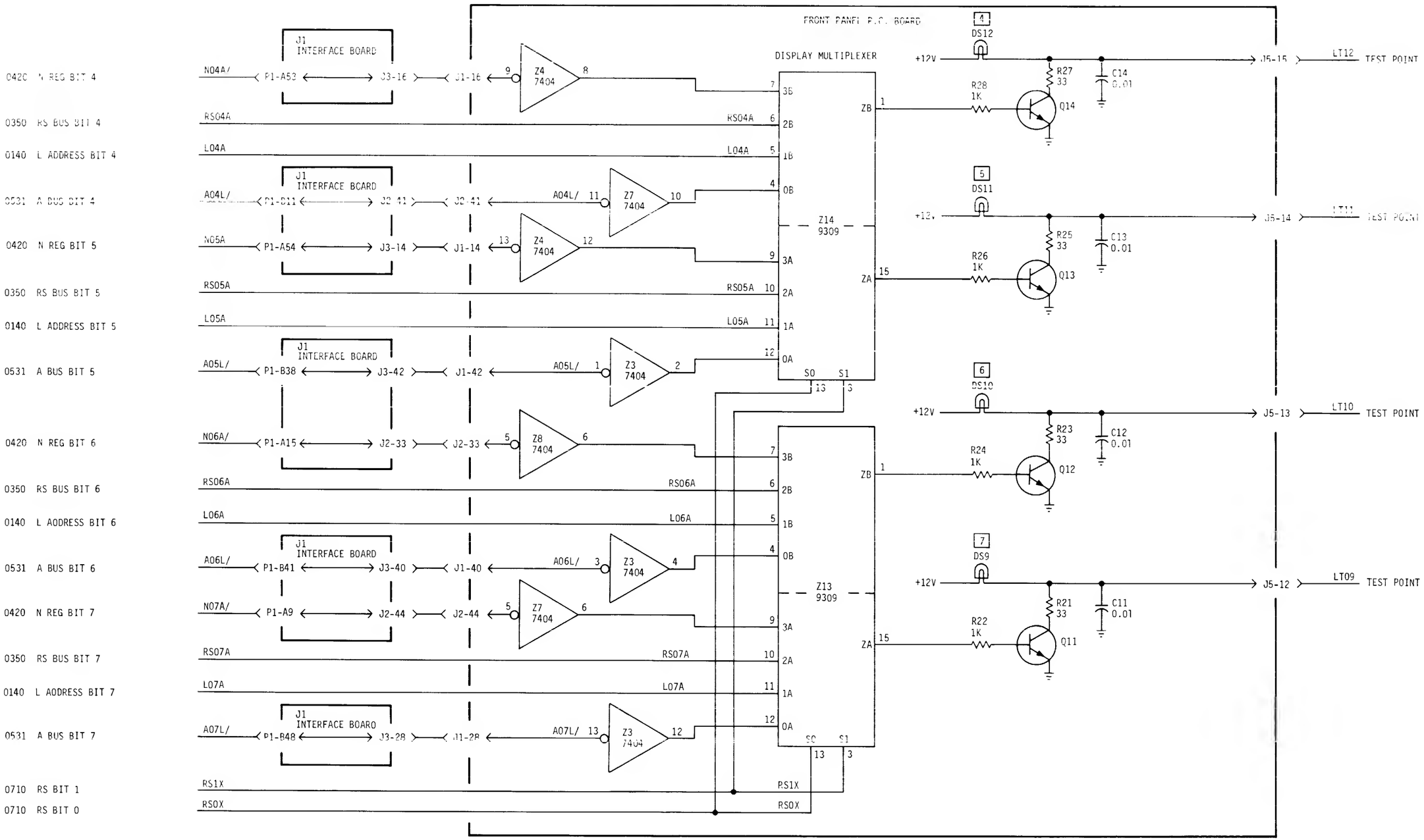
RTCK/ RESET INTERRUPT, 0630

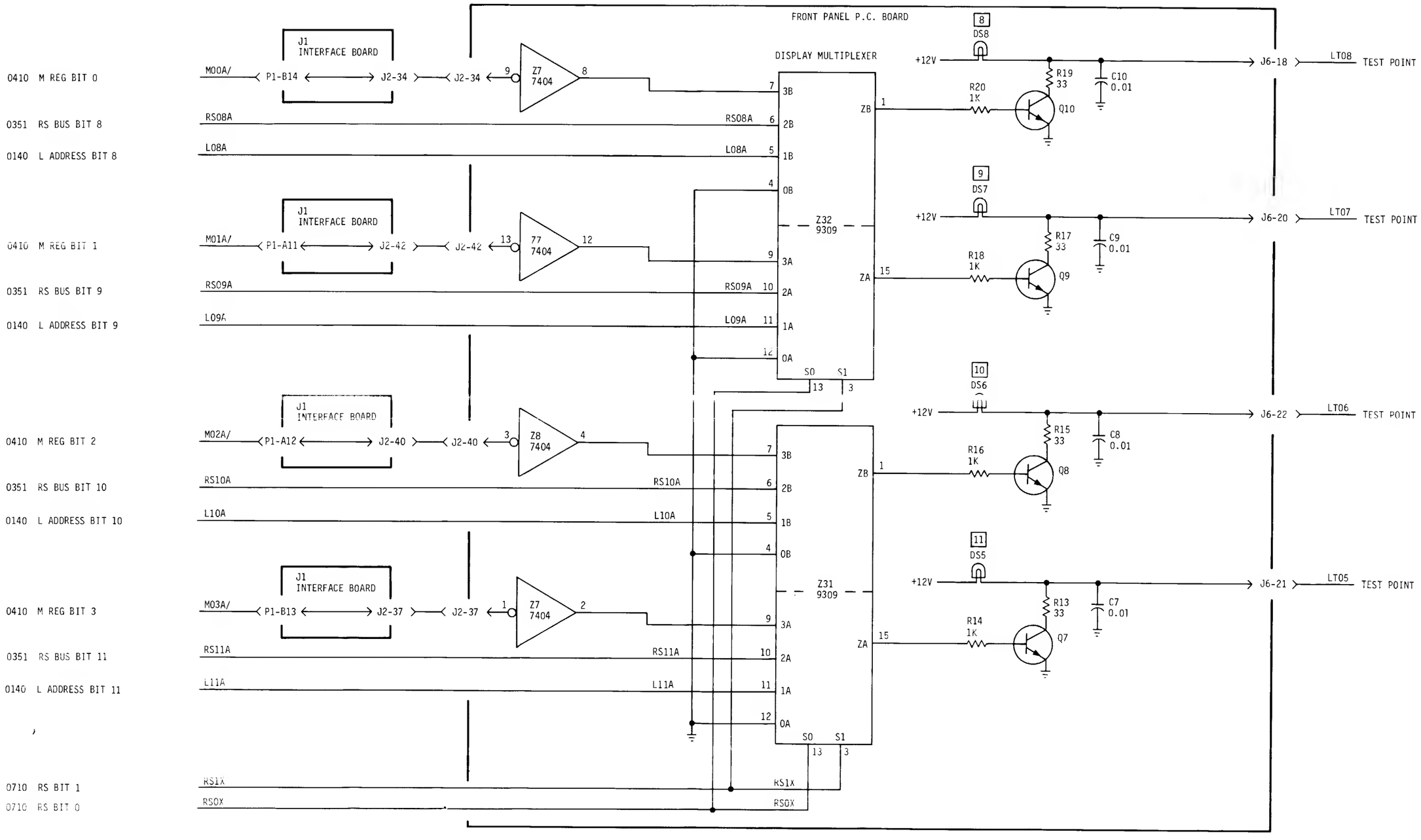


FRONT PANEL DISPLAY INDICATORS BITS 0-3

FRONT PANEL P.C. BOARD
AND J1 INTERFACE BOARD
0710

FRONT PANEL DISPLAY INDICATORS BITS 4-7

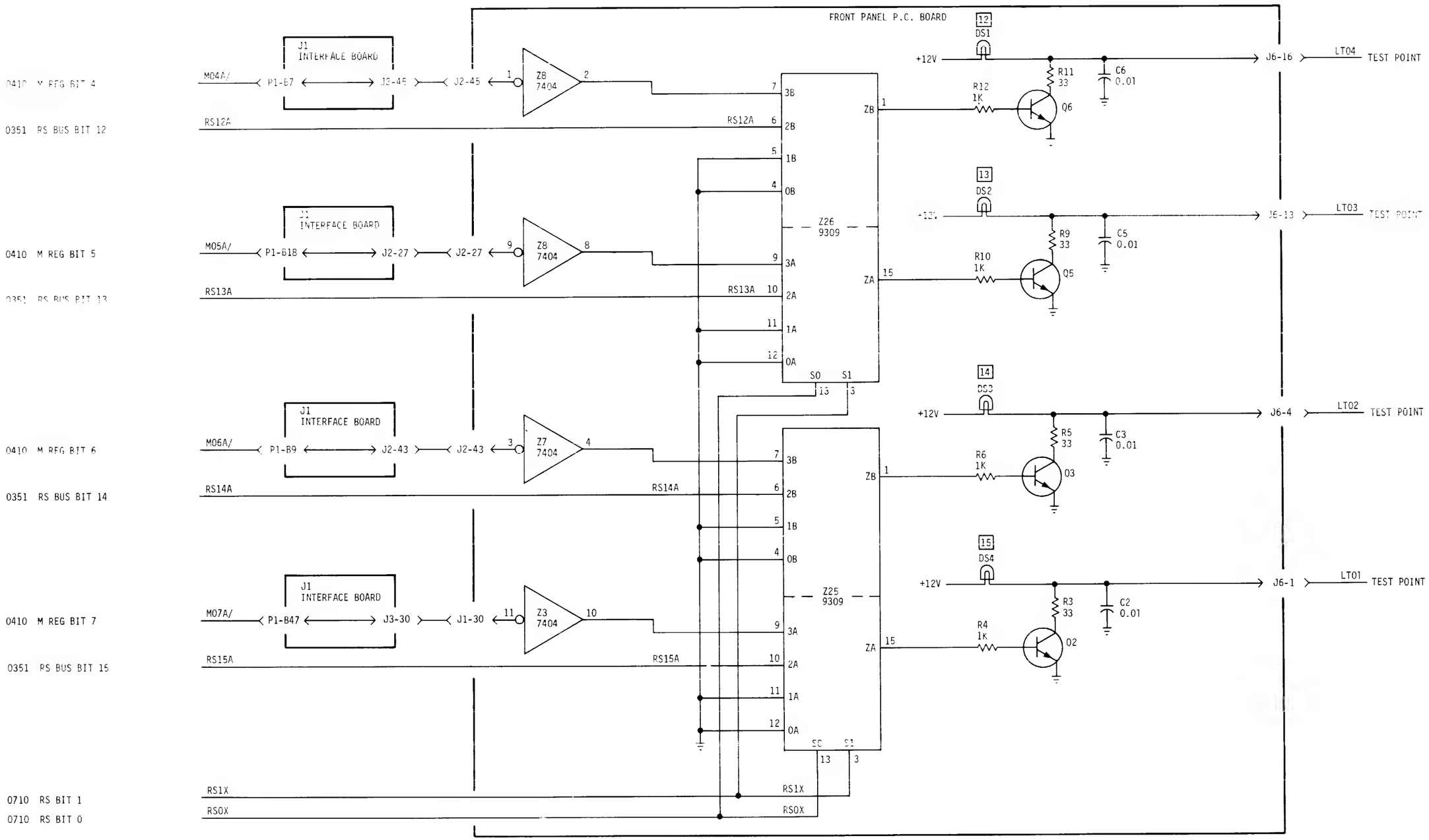




FRONT PANEL DISPLAY INDICATORS BITS 8-11

FRONT PANEL P.C. BOARD
0730

FRONT PANEL DISPLAY INDICATORS BITS 12-15



PG iv INPUT DATA BIT D

PG iv INPUT DATA BIT 1

PG iv INPUT DATA BIT 2

PG iv INPUT DATA BIT 3

PG iv INPUT DATA BIT 4

PG iv INPUT DATA BIT 5

PG iv INPUT DATA BIT 6

PG iv INPUT DATA BIT 7

0372 SEL UNCOMP INPUT DATA

0370 SUBTRACT COMMAND

0430 T REG BIT 0 - 3

0431 T REG BIT 4 - 7

0810 SAVE CONTENTS OF OD REG

0550 PULL-UP 1

0361 R REG BIT 4

0361 R REG BIT 5

0361 R REG BIT 6

0230 DATA CLOCK

0372 EXTERNAL I/O COMMAND

PG iv MASTER RESET

IDOO/ P1-B32

ID01/ P1-A6D

ID02/ P1-B62

ID03/ P1-A62

ID04/ P1-A32

ID05/

ID06/ P1-A61

ID07/ P1-B60

IOHT J3-28

SBXX/ J3-29

TOOX/-T03X/

T04X/-TD7X/

IOSV

PUL1

RO4X/ J2-9

RD5X J3-42

RO6X J2-30

CLK1/ J3-36

EXID/ J2-37

MRST/ P1-B44

+5V

Z7 200 Z7 2DO Z7 200 Z7 200

Z7 300 Z7 300 Z7 3DO Z7 300

Z8 200 Z8 20D Z8 200 Z8 200

Z8 300 Z8 300 Z8 300 Z8 30C

INPUT DATA BUS GATES

4J 7486 — ID00G, ID01G, IO02G, ID03G

5J 7486 — ID04G, ID05G, ID06G, ID07G

9J 74H00

ID00G-ID03G

ID04G-IDD7G

ID00G-ID03G INPUT DATA BITS 0-3, 0510

ID04G-ID07G INPUT OATA BITS 4-7, 0511

OD REGISTER

3C 9308

TOOX/ T01X/ T02X/ T03X/ — P1-B39 OD00/ OUTPUT OATA BIT D, PG iv; P1-B1D OD01/ OUTPUT OATA BIT 1, PG iv; P1-A26 OD02/ DUTPUT DATA BIT 2, PG iv; P1-B58 OD03/ DUTPUT DATA BIT 3, PG iv

T04X/ T05X/ T06X/ T07X/ — P1-B37 OD04/ DUTPUT DATA BIT 4, PG iv; P1-A10 0005/ OUTPUT DATA BIT 5, PG iv; P1-B26 OD06/ OUTPUT DATA BIT 6, PG iv; P1-A58 OD07/ OUTPUT OATA BIT 7, PG iv

IC REGISTER 2D 9308

RO4A RO5X RO6X — Q3 Q2 Q1 Q0

1C 7437 — IO1X/, IO2X/, IO3X/

7D 74H10 — IOSV SAVE CONTENTS OF OD REG, 0810

P1-B31 IO1X/ I/O CONT REG 1, PG iv

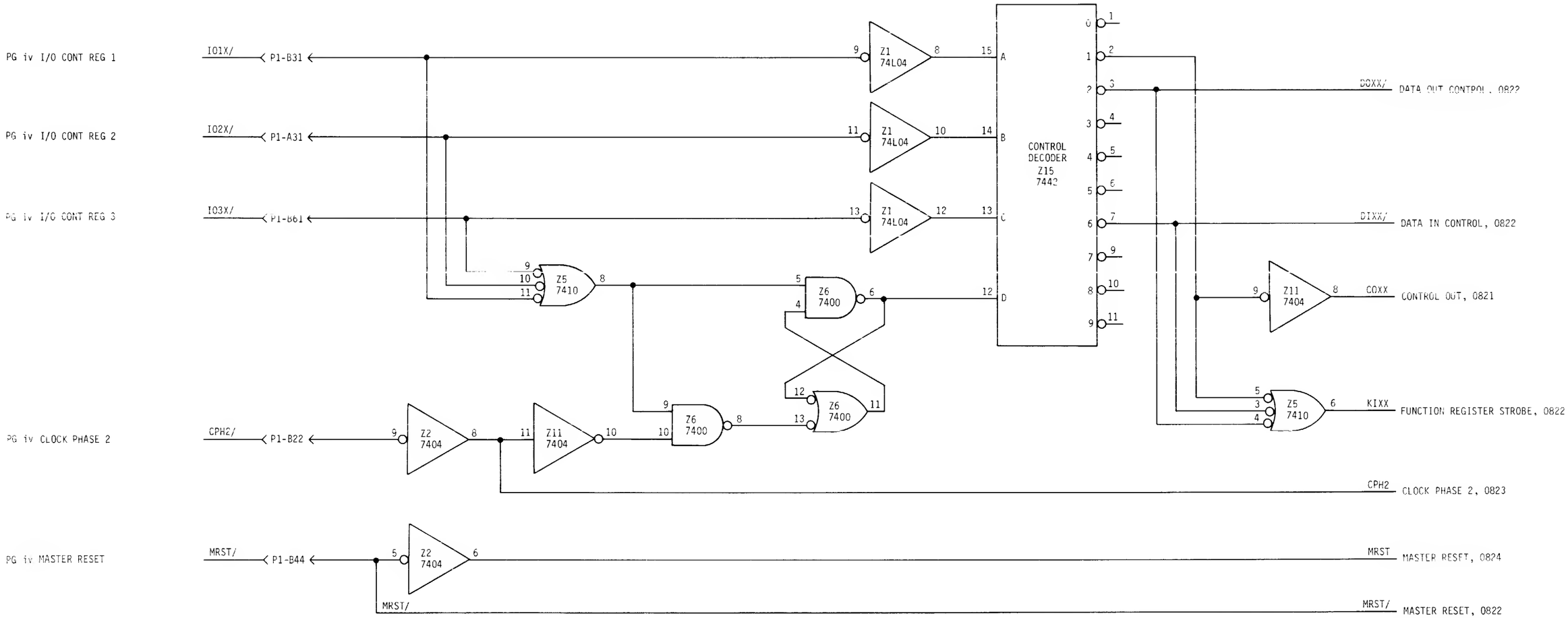
P1-A31 IO2X/ I/O CONT REG 2, PG iv

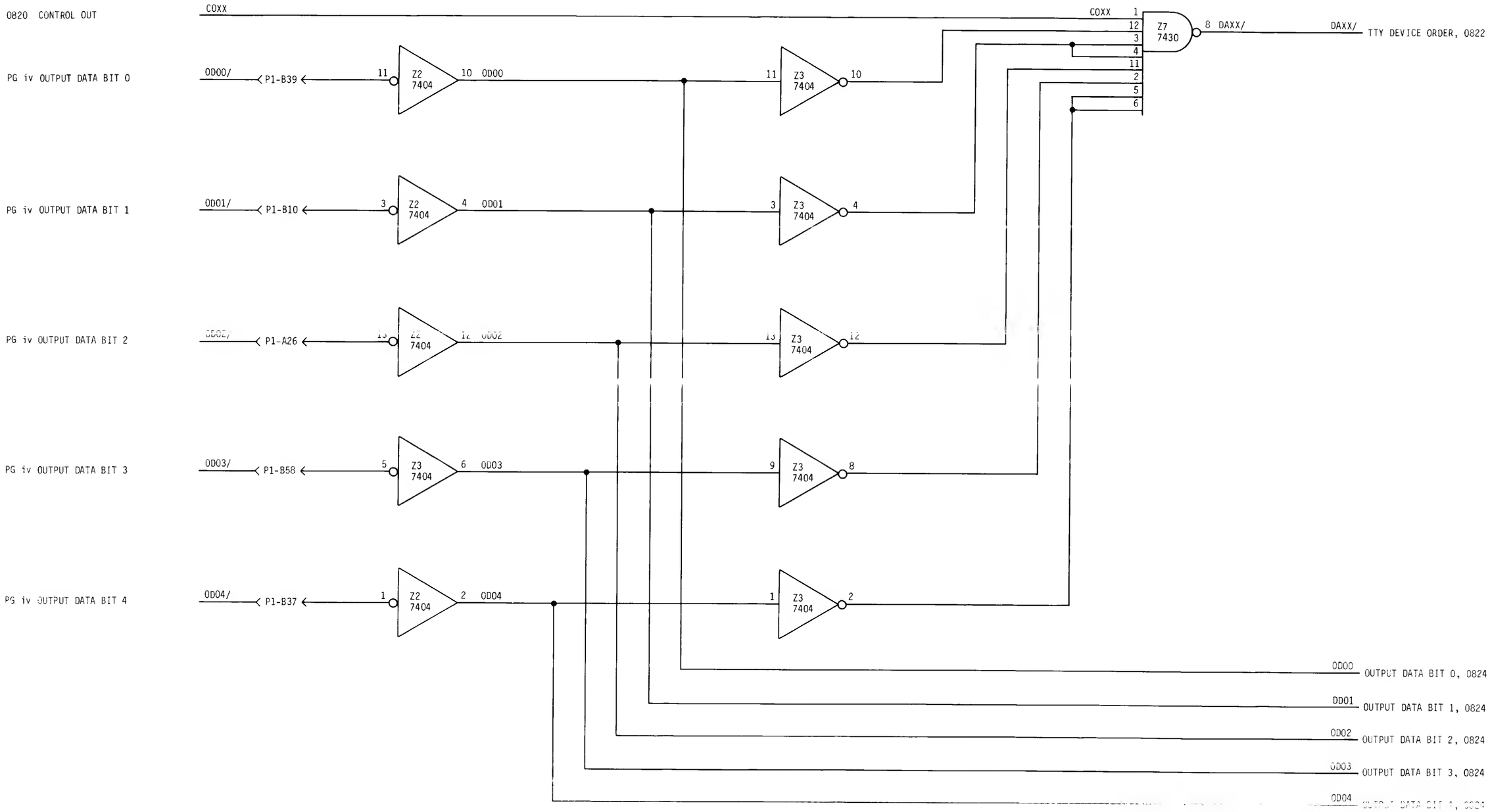
P1-B61 ID3X/ I/O CONT REG 3, PG iv

ID3X/ I/O CONT REG 3, 0374

INPUT DATA BUS GATES, IC REGISTER AND OD REGISTER

J3 DATA BOARD
0810

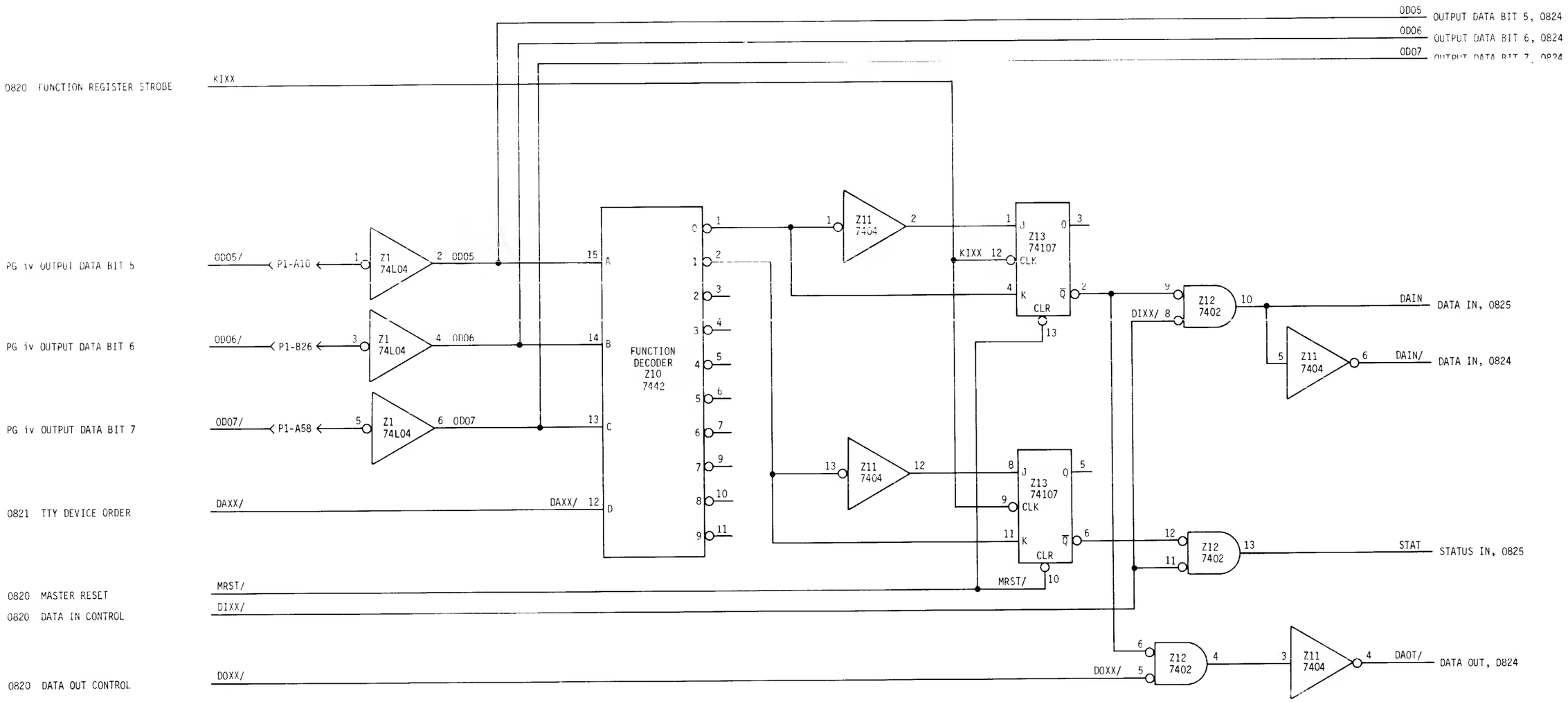

PG iv I/O CONT REG 1
IO1X/
P1-B31
PG iv I/O CONT REG 2
IO2X/
P1-A31
PG iv I/O CONT REG 3
IO3X/
P1-B61
Z1 74L04
Z5 7410
Z6 7400
CONTROL DECODER Z15 7442
DOXX/
DATA OUT CONTROL, 0822
DIXX/
DATA IN CONTROL, 0822
Z11 7404
COXX
CONTROL OUT, 0821
KIXX
FUNCTION REGISTER STROBE, 0822
PG iv CLOCK PHASE 2
CPH2/
P1-B22
Z2 7404
CPH2
CLOCK PHASE 2, 0823
PG iv MASTER RESET
MRST/
P1-B44
MRST
MASTER RESET, 0824
MRST/
MASTER RESET, 0822

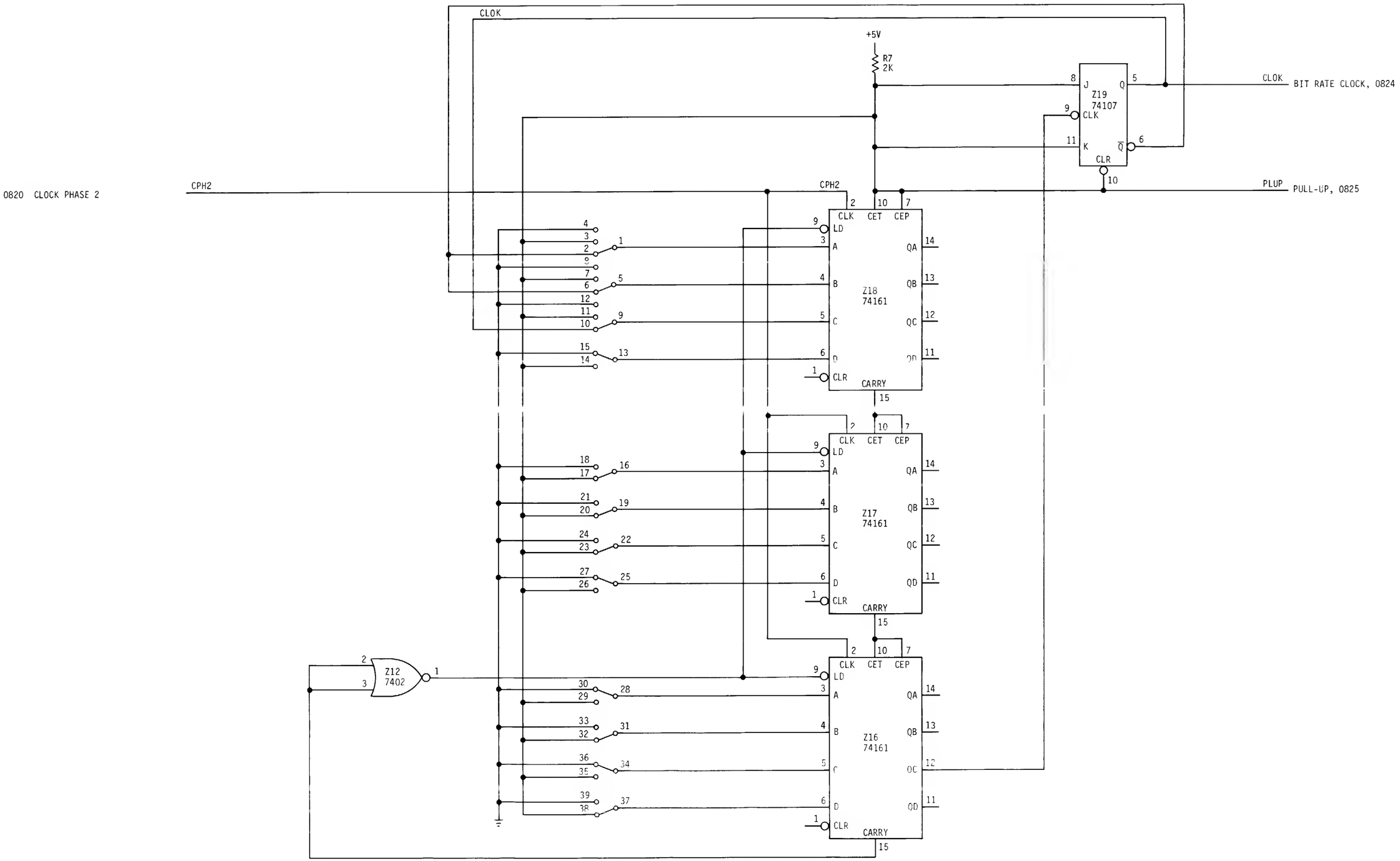


TTY CONTROLLER - ADDRESS DECODER

J1 INTERFACE BOARD
0821

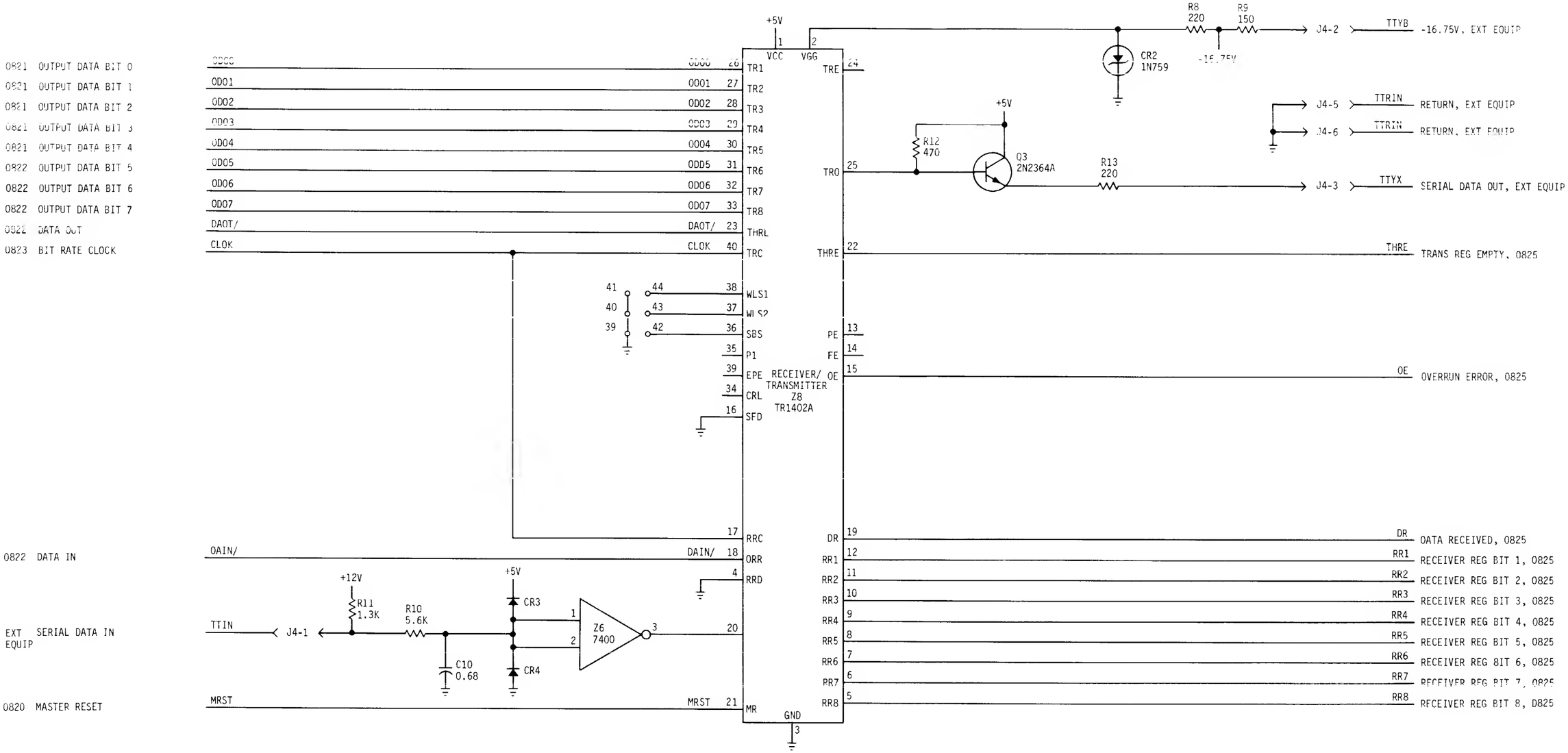
TTY CONTROLLER - FUNCTION DECODER

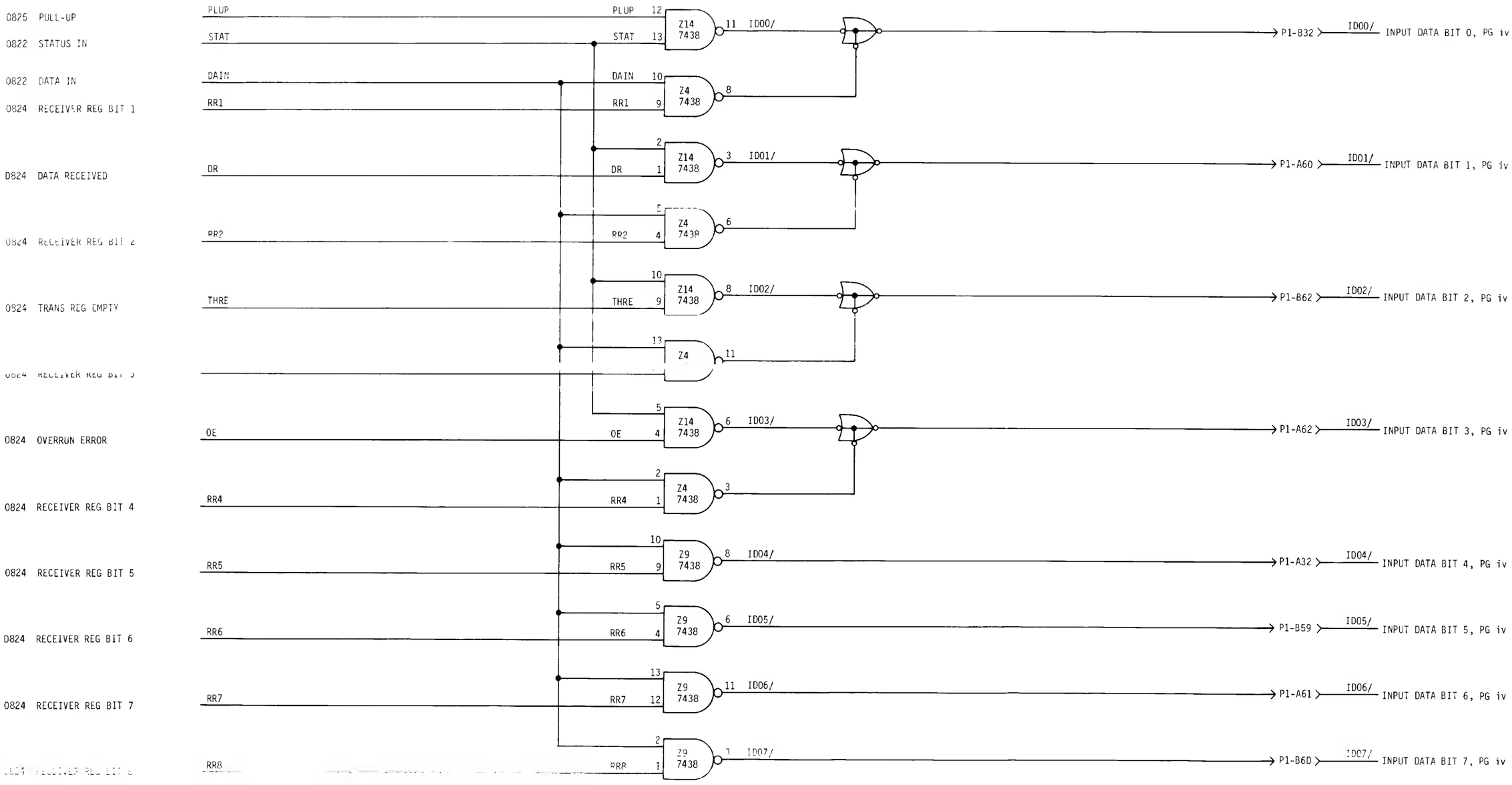




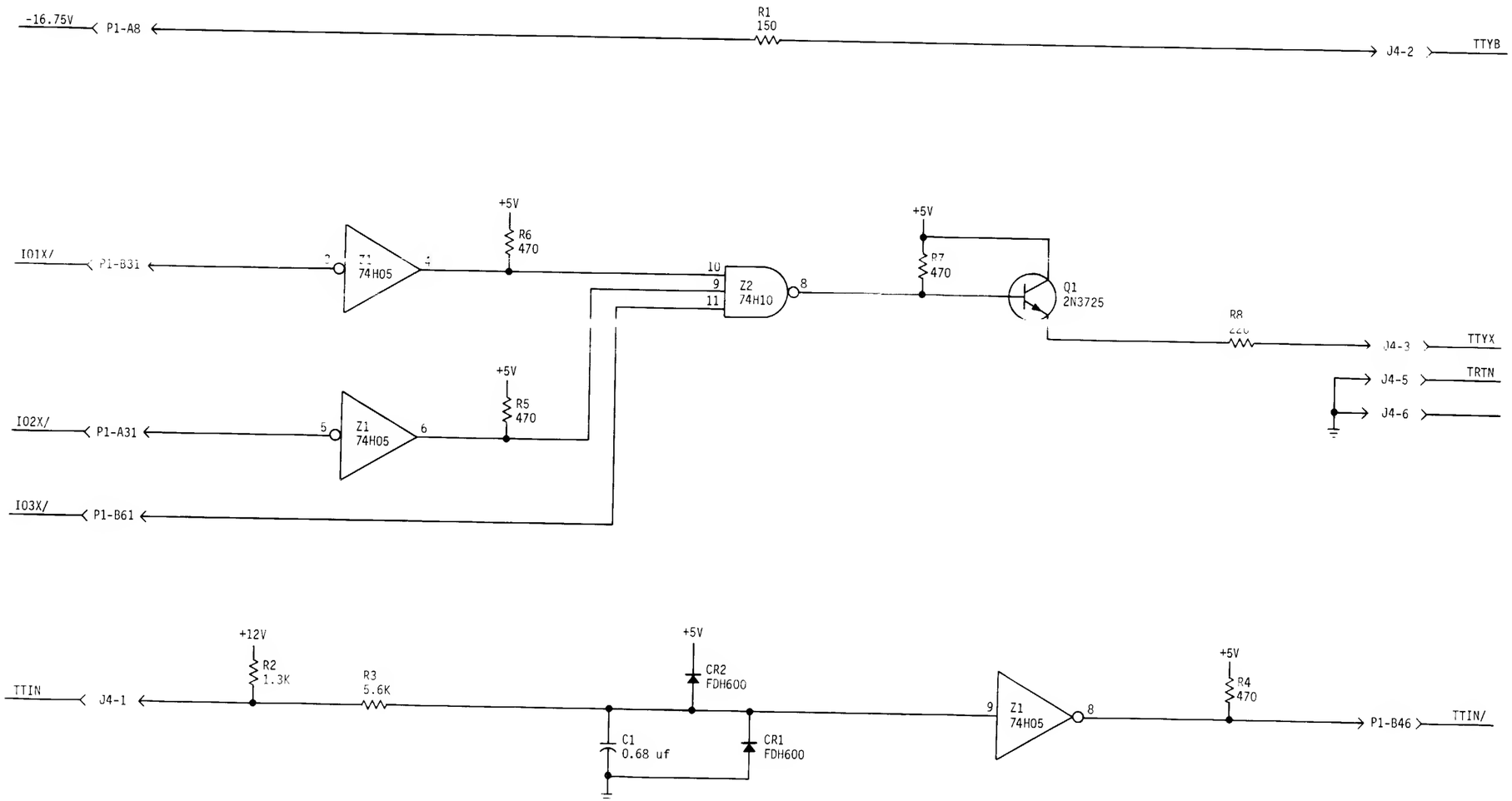
TTY CONTROLLER - BIT RATE CLOCK GENERATOR

J1 INTERFACE BOARD
0823


0821 OUTPUT DATA BIT 0
0821 OUTPUT DATA BIT 1
0821 OUTPUT DATA BIT 2
0821 OUTPUT DATA BIT 3
0821 OUTPUT DATA BIT 4
0822 OUTPUT DATA BIT 5
0822 OUTPUT DATA BIT 6
0822 OUTPUT DATA BIT 7
0822 DATA OUT
0823 BIT RATE CLOCK
ODD0
ODD1
ODD2
ODD3
ODD4
ODD5
ODD6
ODD7
DAOT/
CLOK
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
THRL
TRC
+5V
VCC
VGG
TRE
TRO
THRE
R8 220
R9 150
-16.75V
CR2 1N759
J4-2
TTYB
-16.75V, EXT EQUIP
J4-5
TTRIN
RETURN, EXT EQUIP
J4-6
TTRIN
RETURN, EXT EQUIP
R12 470
Q3 2N2364A
R13 220
J4-3
TTYX
SERIAL DATA OUT, EXT EQUIP
TRANS REG EMPTY, 0825
41
40
39
44
43
42
WLS1
WLS2
SBS
P1
EPE
CRL
SFD
RECEIVER/ TRANSMITTER Z8 TR1402A
PE
FE
OE
OVERRUN ERROR, 0825
RRC
ORR
RRD
DAIN/
OAIN/
0822 DATA IN
EXT SERIAL DATA IN EQUIP
TTIN
J4-1
+12V
R11 1.3K
R10 5.6K
C10 0.68
CR3
CR4
Z6 7400
MRST
0820 MASTER RESET
MR
GND
DR
OATA RECEIVED, 0825
RR1
RR2
RR3
RR4
RR5
RR6
RR7
RR8
RECEIVER REG BIT 1, 0825
RECEIVER REG BIT 2, 0825
RECEIVER REG BIT 3, 0825
RECEIVER REG BIT 4, 0825
RECEIVER REG BIT 5, 0825
RECEIVER REG BIT 6, 0825
RECEIVER REG BIT 7, 0825
RECEIVER REG BIT 8, D825

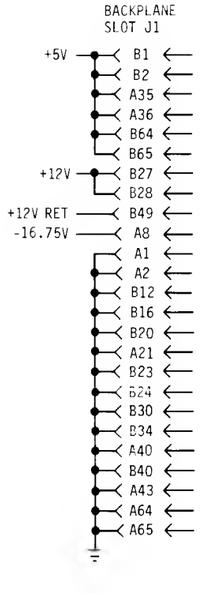


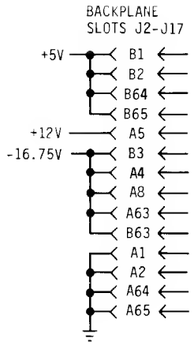
TTY CONTROLLER - INPUT DATA GATES

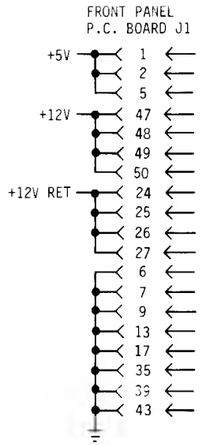


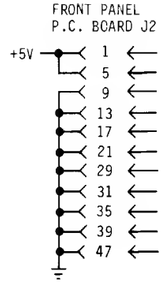
SERIAL TTY INTERFACE

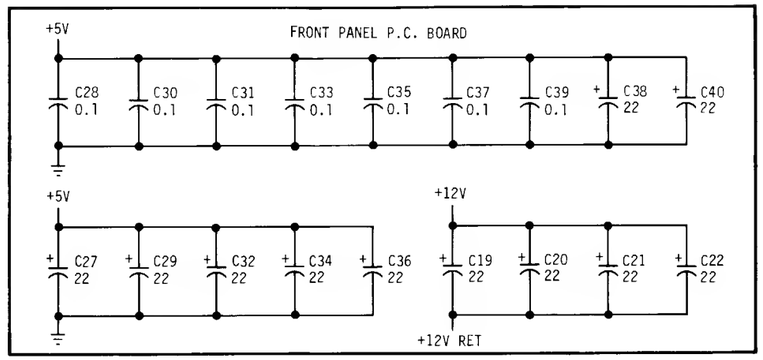
0830
J1 INTERFACE BOARD

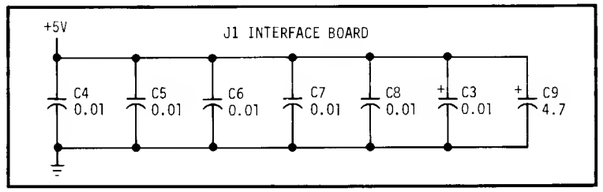


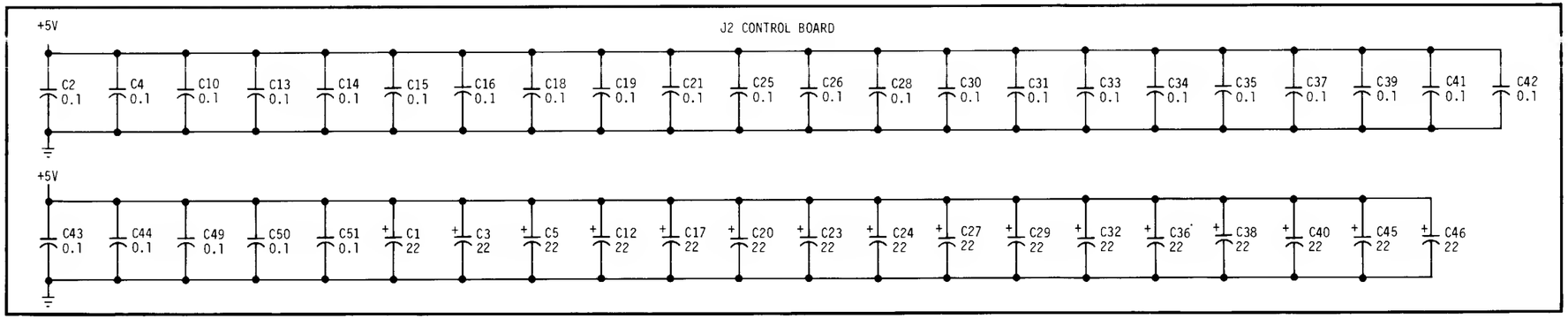


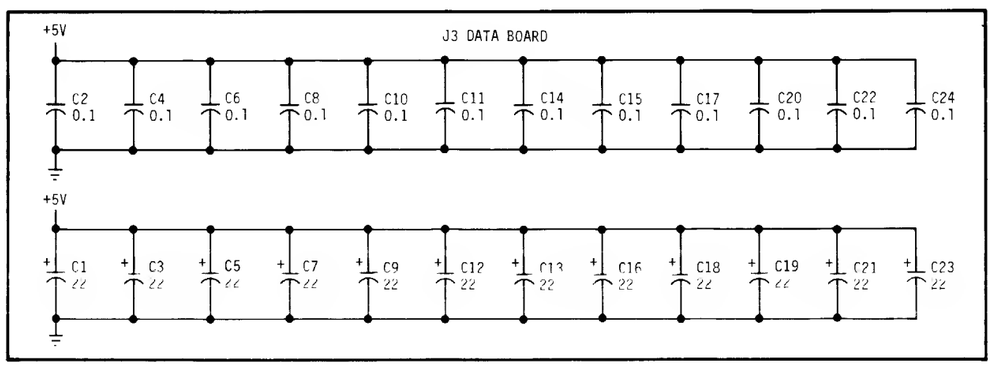


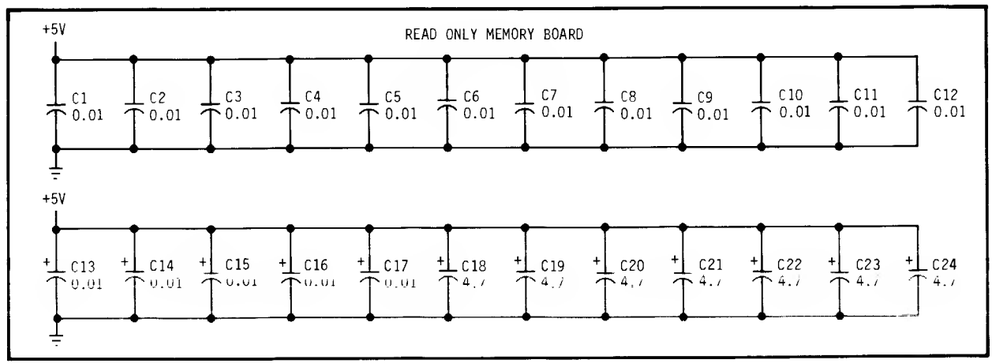








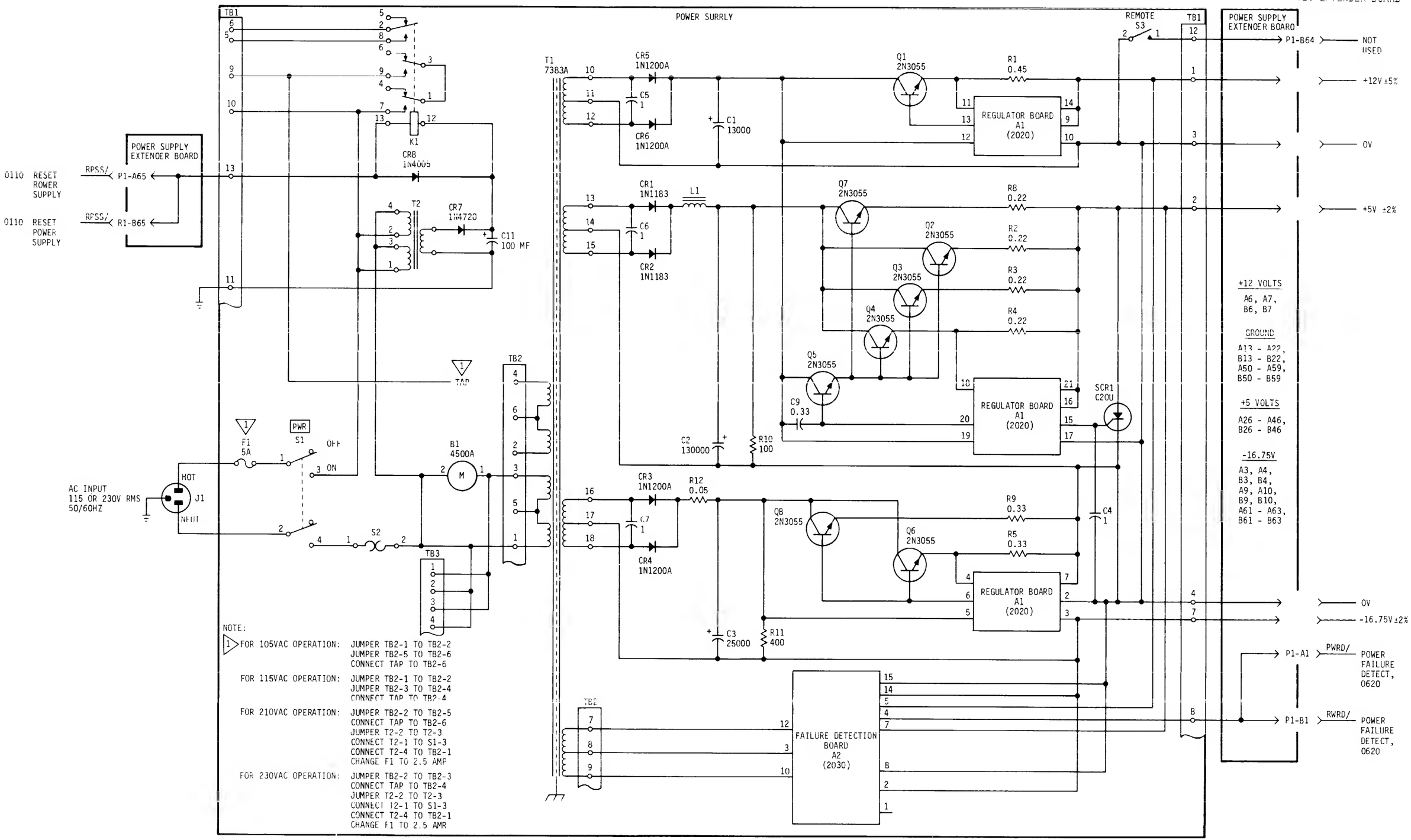




POWER DISTRIBUTION

POWER SUPPLY CIRCUIT

2010
POWER SUPPLY AND
I18 EXTENDER BOARD



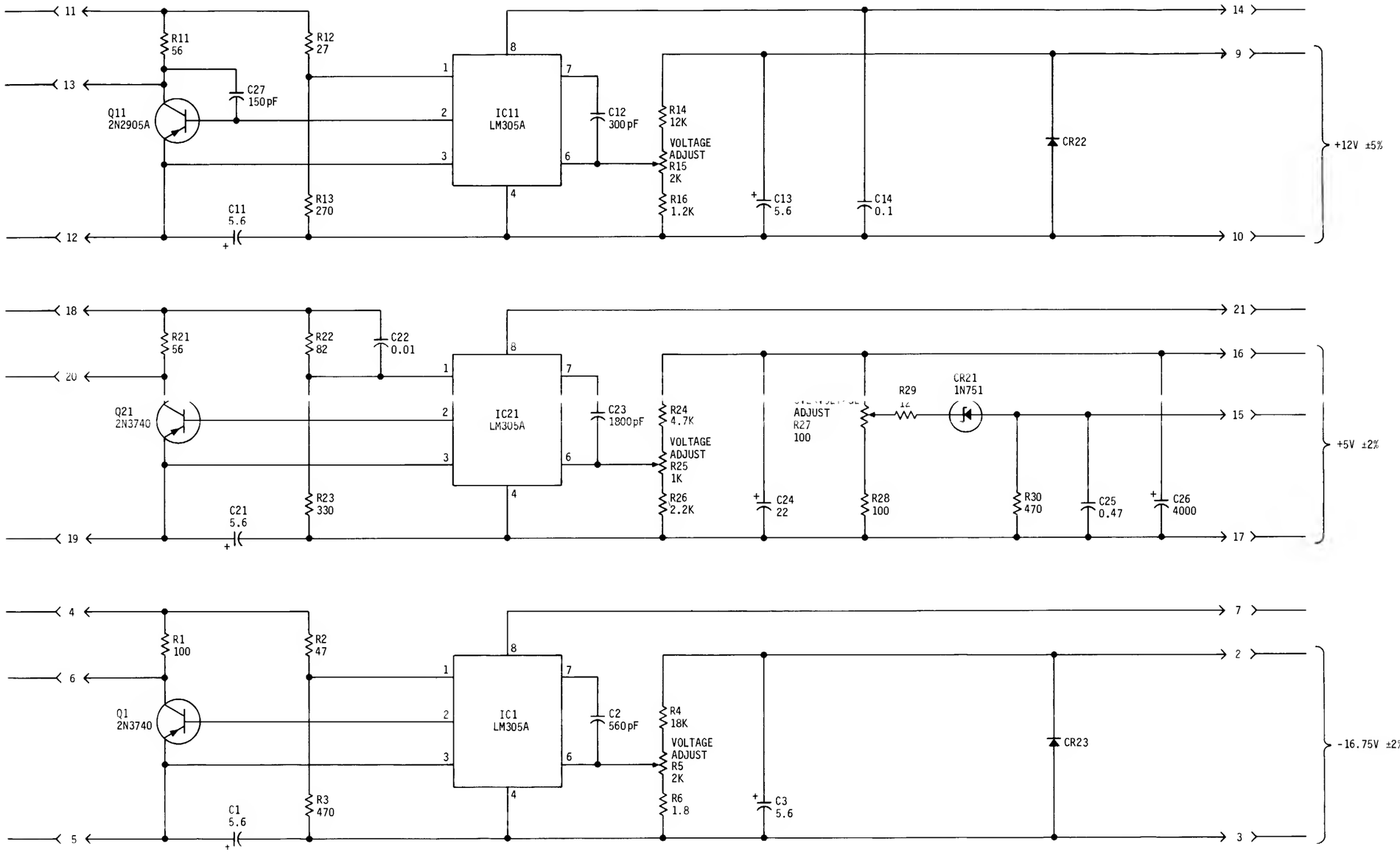
NOTE:

1. FOR 105VAC OPERATION:
   - JUMPER TB2-1 TO TB2-2
   - JUMPER TB2-5 TO TB2-6
   - CONNECT TAP TO TB2-6

   FOR 115VAC OPERATION:
   - JUMPER TB2-1 TO TB2-2
   - JUMPER TB2-3 TO TB2-4
   - CONNECT TAP TO TB2-4

   FOR 210VAC OPERATION:
   - JUMPER TB2-2 TO TB2-5
   - CONNECT TAP TO TB2-6
   - JUMPER T2-2 TO T2-3
   - CONNECT T2-1 TO S1-3
   - CONNECT T2-4 TO TB2-1
   - CHANGE F1 TO 2.5 AMP

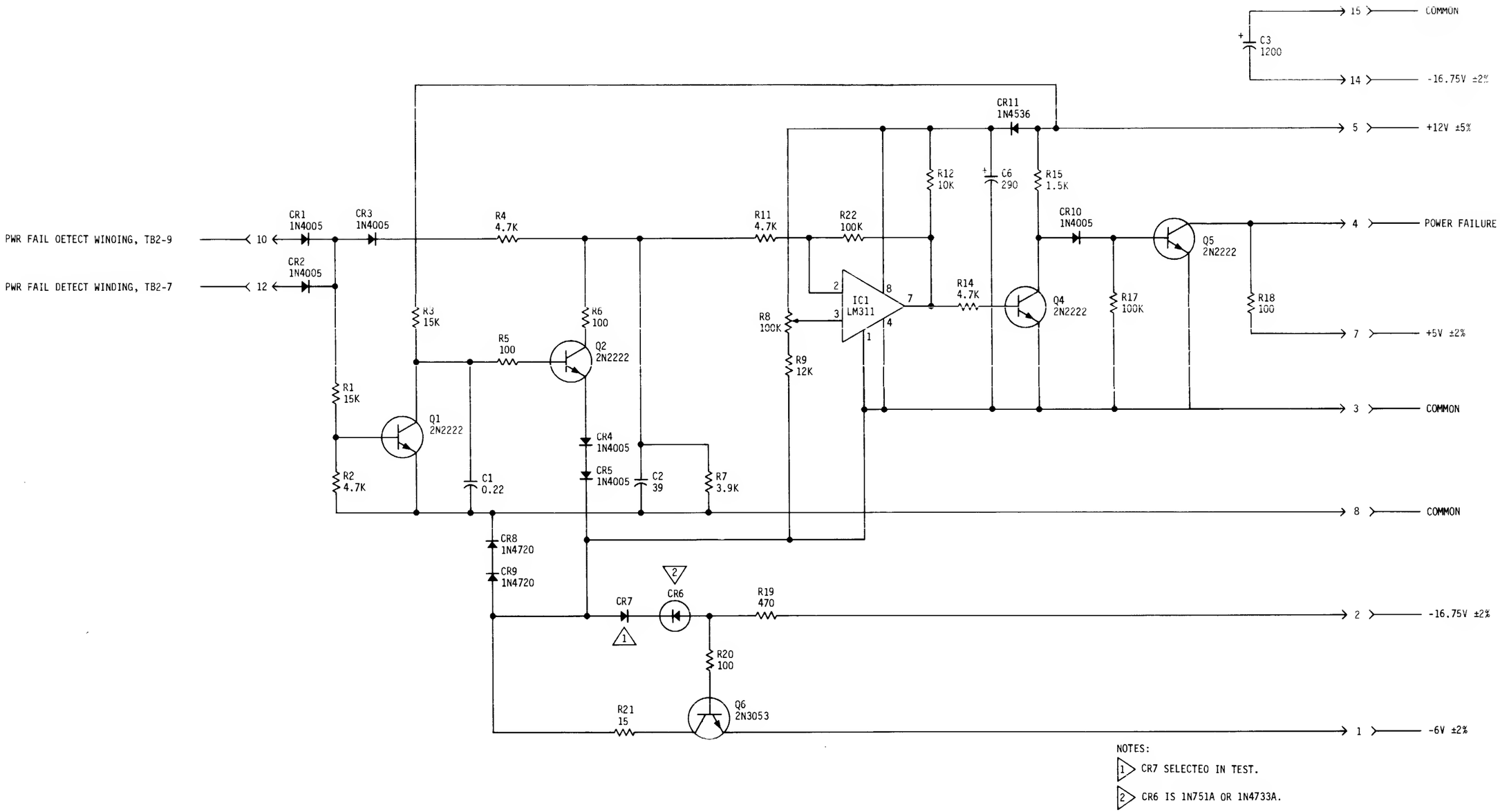
   FOR 230VAC OPERATION:
   - JUMPER TB2-2 TO TB2-3
   - CONNECT TAP TO TB2-4
   - JUMPER T2-2 TO T2-3
   - CONNECT T2-1 TO S1-3
   - CONNECT T2-4 TO TB2-1
   - CHANGE F1 TO 2.5 AMR



REGULATOR CIRCUITS

J2 REGULATOR BOARD A1
2020

FAILURE DETECTION CIRCUIT



NOTES:

1. CR7 SELECTEO IN TEST.
2. CR6 IS 1N751A OR 1N4733A.